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OUTLINING AND SHADING GENERATION FOR A COLOR TELEVISION DISPLAY

by

DONALD FARNESS HANSON

June, 1972

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I. INTRODUCTION

The work described here is the second version of the Automatic Tricolor Cartograph (ATC). Phase one of the project was completed in 1968. At that time it was decided that certain improvements could and should be made on the machine. These improvements were

(a) to alleviate a color bleeding problem,

(b) to remove a moire pattern that plagued the display,

and (c) to add shades of gray capability.

The solution of these problems is the subject of this work.

A brief description of the original system will be included here, but for a complete discussion of Phase I, the reader should read the thesis "A Tricolor Cartograph" [1]. The machine as described in [1] will be referred to as the ATC - Mark I. The additions and changes described here were made on the ATC - Mark I. The machine as described in this report will be referred to as the ATC - Mark II. A photograph of the ATC - Mark II is shown in Figure 1. In general terms, the ATC - Mark I performed the same functions as the ATC - Mark II now does. In general terms, then, the machine will be referred to simply as the ATC.

The ATC is a color graphics display terminal capable of "drawing" and displaying color graphical information. The operator is able to draw an outline on the display screen and fill it in with color. The machine uses hard-wired algorithms for achieving this end; it is entirely self-enclosed and no digital computer hookups are needed.

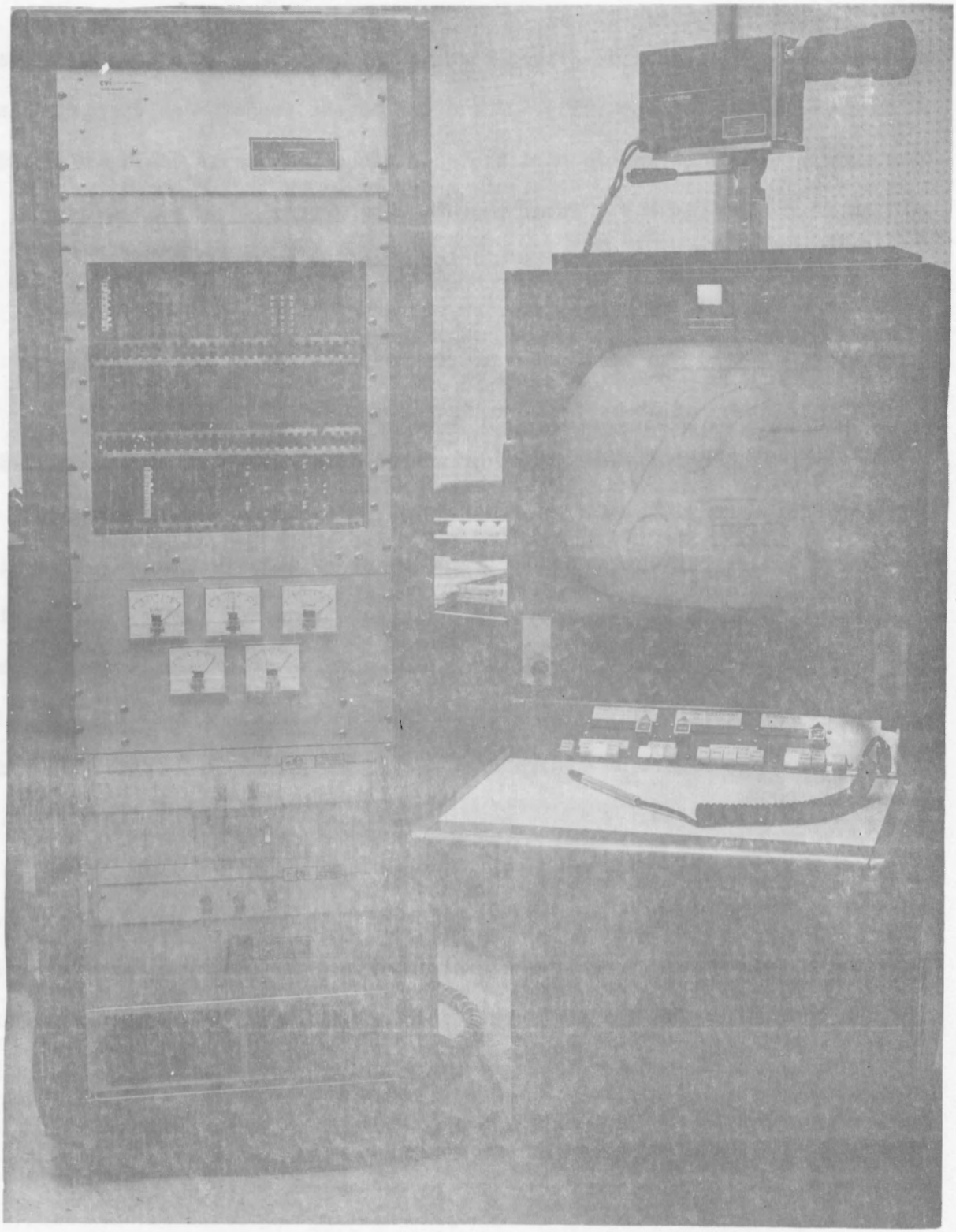


Figure 1. The Automatic Tricolor Cartograph - Mark II (ATC - Mark II)

The basic components of the ATC are

(1) an analog disc,

(2) a switch control panel,

(3) a light pen,

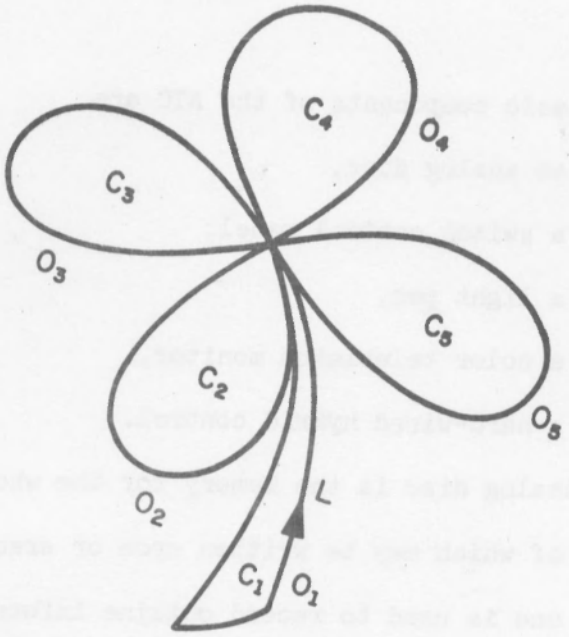
(4) a color television monitor,

and (5) a hard-wired hybrid control.

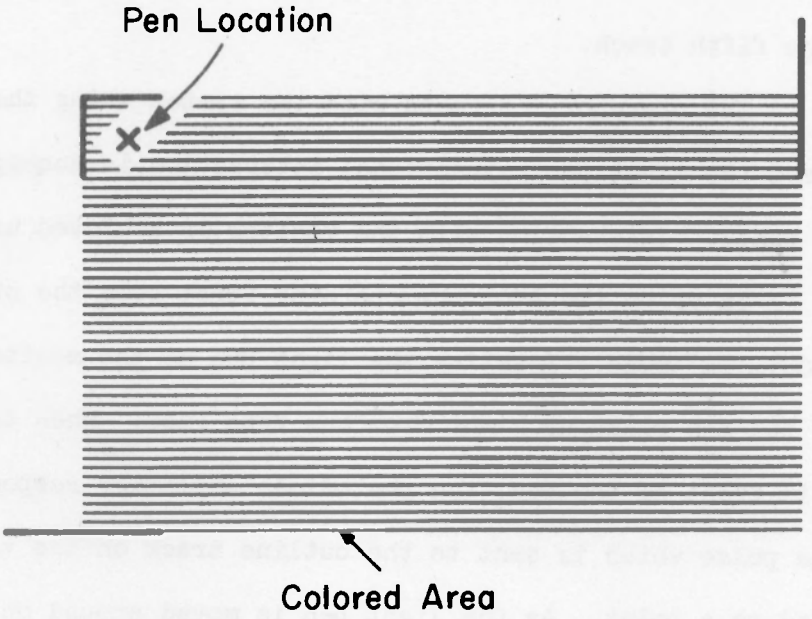
The analog disc is the memory for the whole system. It has five channels, four of which may be written upon or erased at will. Of these four channels, one is used to record outline information, and three are used to record color information. All four of these channels are continuously "played back" on the monitor. The sync information is permanently recorded upon the fifth track.

The operator interacts with the system using the switch control panel and the light pen. Functional interaction is accomplished using the switch panel. Interaction with the monitor is achieved using the light pen.

In using the ATC, the operator first sets the switch panel to the "DRAW OUTLINE" mode. Pointing the light pen at the monitor, a photodiode inside the pen picks up light from the tube face. When the scanned beam moves in front of the pen, the photodiode amplifier responds with a large voltage pulse which is sent to the outline track on the video disc and is recorded as a point. As the light pen is moved around on the face of the monitor a line drawing results. This line drawing L [see Figure 2(a)] can be arbitrary, and, in general, can be broken up into subsets C_n of open or closed regions whose boundaries may be shared but whose "areas" are not criss-crossed with any other lines. The boundary of each C_n is here called the "outline" O_n. Next, the operator sets the pen to the "COLOR" mode and



(a) Line Drawing L Broken into Regions C_n with Outline O_n



(b) An Open Line Drawing that Will Be Colored for Pen Location as Shown

Figure 2. Line Drawings

the color selector switches to the desired color, "RED", "GREEN", "BLUE", or any mixture of these. He then places the pen on the screen somewhere inside of the outline O_n, and the coloring logic automatically generates a waveform that corresponds to the inside of the outline O_n that he has indicated. This waveform is then sent to the disc where it is chopped and written upon those video disc channels corresponding to the selected colors. This signal is then read and sent to the monitor. If the outline O_n is closed, then the entire area bounded by the outline may be filled in. If, however, the "outline" O_n is open, the coloring logic decides if enough information is known to "fill it in" [see Figure 2(b)]. After coloring, new outlines may be drawn and colored in. In this way, color may be added to already present color. Selected automatic erasure and point by point writing and erasure are also possible in addition to the automatic coloring described above.

For a detailed discussion of the ATC - Mark I, see [1].

II. THE DESIGN PHILOSOPHY FOR THE ATC - MARK II

Before presenting a discussion of the problems with the ATC - Mark I and the design philosophy for the ATC - Mark II, a discussion of the ATC television system will be given.

A. Fundamentals of the ATC Video and Synchronizing Signals

A very brief summary of the ATC video and synchronizing signals will be given here. References [2], [3] and [4] deal with standard television in much more detail.

1. The Monitor

In the Tricolor Cartograph (ATC) as with most American television systems, a complete picture, called a frame, consists of 525 horizontally scanned lines. Each frame consists of two fields. An odd numbered line belongs to the odd field, and an even numbered line belongs to the even field. Each field scans the entire height of the monitor in such a manner that a scan line from the odd field is interlaced between two from the even. In this way, visible flicker due to phosphor decay rates is avoided.

One line is scanned in about 63.5 μsec., one field in about 16 2/3 msec. and one frame in about 33 1/3 msec. At these rates, 30 frames are scanned per second which is fast enough to give the illusion of smooth movement.

It is worthwhile to note that adjacent lines appearing on the CRT face are 16 2/3 msec. apart in time, whereas every other line is just 63.5 μsec apart.

2. The Disc

The various components of the ATC are synchronized using Horizontal Drive (HD) and Vertical Drive (VD) pulses that are derived from a sync signal

recorded on a channel of a video disc that turns once per frame. These pulses initiate scan lines in both the monitor and the camera so that a point on the vidicon image plane is scanned simultaneously with the corresponding point on the monitor. A HD pulse occurs once per line, and a VD pulse occurs once per field. The logical equivalent of HD is LHD and of VD is LVD.

3. The Camera

The output of the camera, called the video signal, is a dynamically scanned representation of a two-dimensional space. Typical video signal voltage waveforms are shown in Figure 3. The blanked portion insures that the retrace cannot be seen during scanning. The sync signal is of very little importance here because the monitor and the camera are synchronized to the disc.

B. A Discussion of the Improvements Incorporated in the ATC - Mark II

At the end of Phase I of the project, the machine possessed three undesirable qualities:

(a) bleeding of color from one outline to another,

(b) vertical stripes in the colored area,

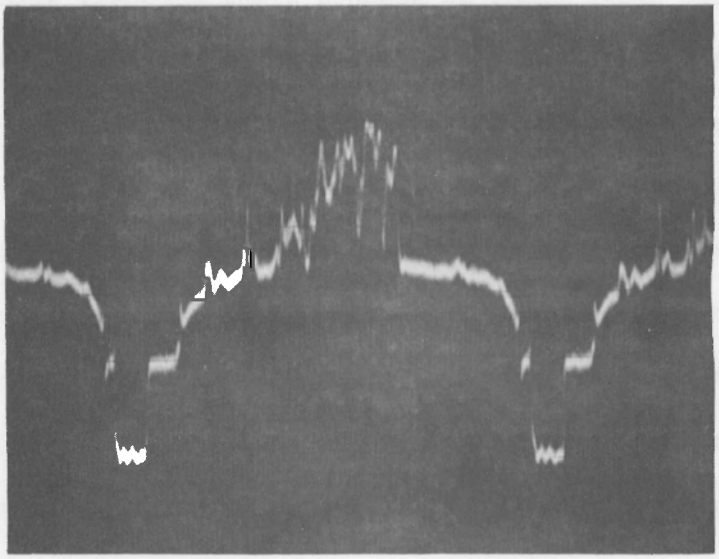
and (c) no shades of gray capability.

1. The Bleeding Problem

When the operator is drawing an outline, he may move the pen by more than one line in a frame's time, thereby leaving gaps. In the case of nested outlines, should a point on an outer outline happen to fall on the same scan line as a gap in the inner outline, the color will "bleed" outside of the inner outline. This effect is discussed in detail in Reference [1].

a. A Discussion of Possible Solutions

Several possibilities exist for solving the bleeding problem. Solutions to this problem that seem reasonable at first become unduly cumbersome



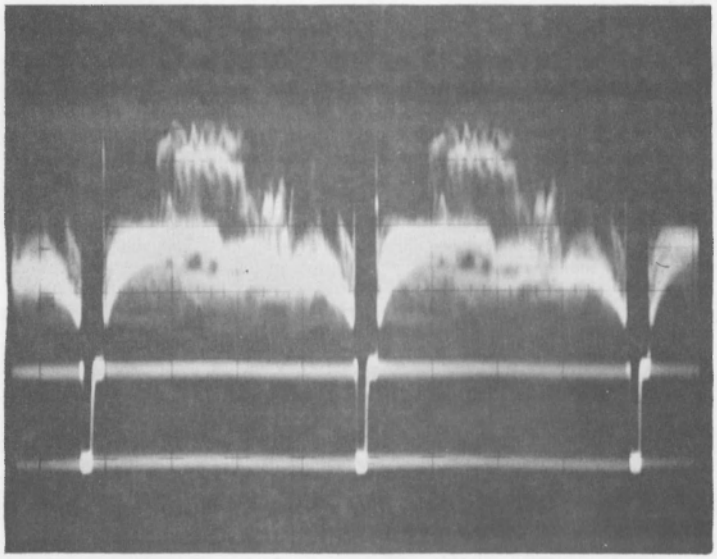


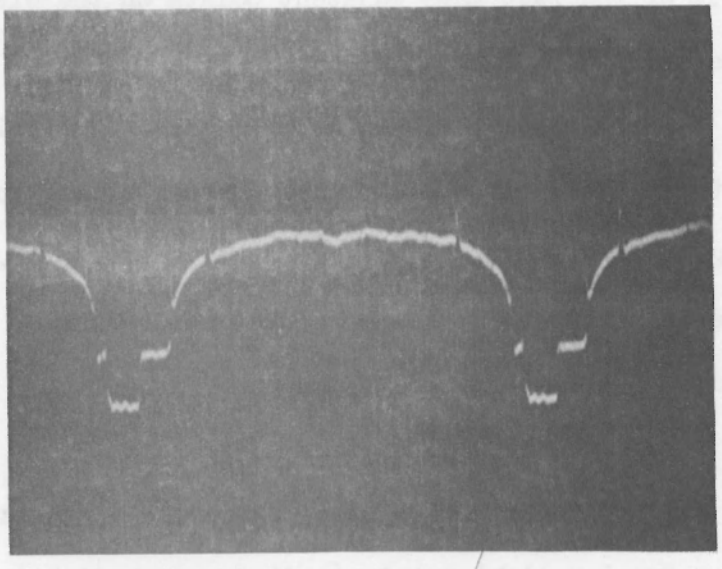
Figure 3. Typical Video Waveforms

after careful thought. One solution would be to develop some sort of gap-filling algorithm. The problem with this, however, is deciding how to define a gap, in view of the fact that adjacent points on the display are sometimes one field apart.

Another solution would be to use a television camera to input outlines instead of the light pen. The camera's video, then, need only be converted to logic. For a suitable video to logic converter, gaps would not appear in the outline. This scheme is the one used here. Camera problems are discussed in the next section.

b. A Discussion of the Camera Problem

In vidicon television cameras, the video signal is curved by a large amount for low light levels (ordinary room light). This is due to a combination of aperture, deflection and focusing effects. At normal room light levels, the video exhibits a decrease in sensitivity from the center to the edge of the line of typically 20%. The camera's automatic gain control emphasizes the curvature by giving the output a higher gain for dark scenes than for well-lit scenes. References [5], [6], and [7] discuss this problem of curvature. Although this variation in curvature is not noticeable on the monitor, it is very noticeable on an oscilloscope display of the video waveform as is shown in Figure 4. The voltage waveform for one line of video is shown in the top photo and for one frame of video in the bottom photo in each (a) and (b). The waveforms in Figure 4(a) result from a simple white outline drawn on a black background while those in Figure 4(b) are the result of a simple black outline drawn on a white background. In each case, the variation in voltage across a line is almost as large as the amplitude of the outline



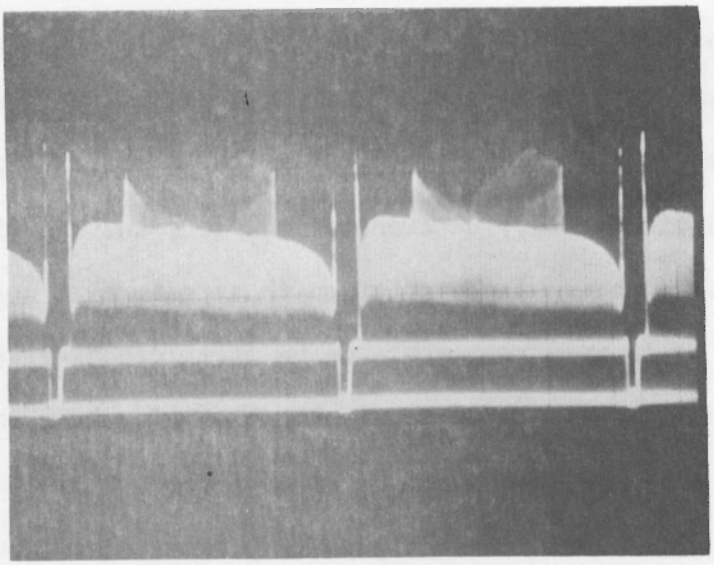


Figure 4. Special Case Video Waveforms

(a) Waveforms of a White Outline on a Black Background

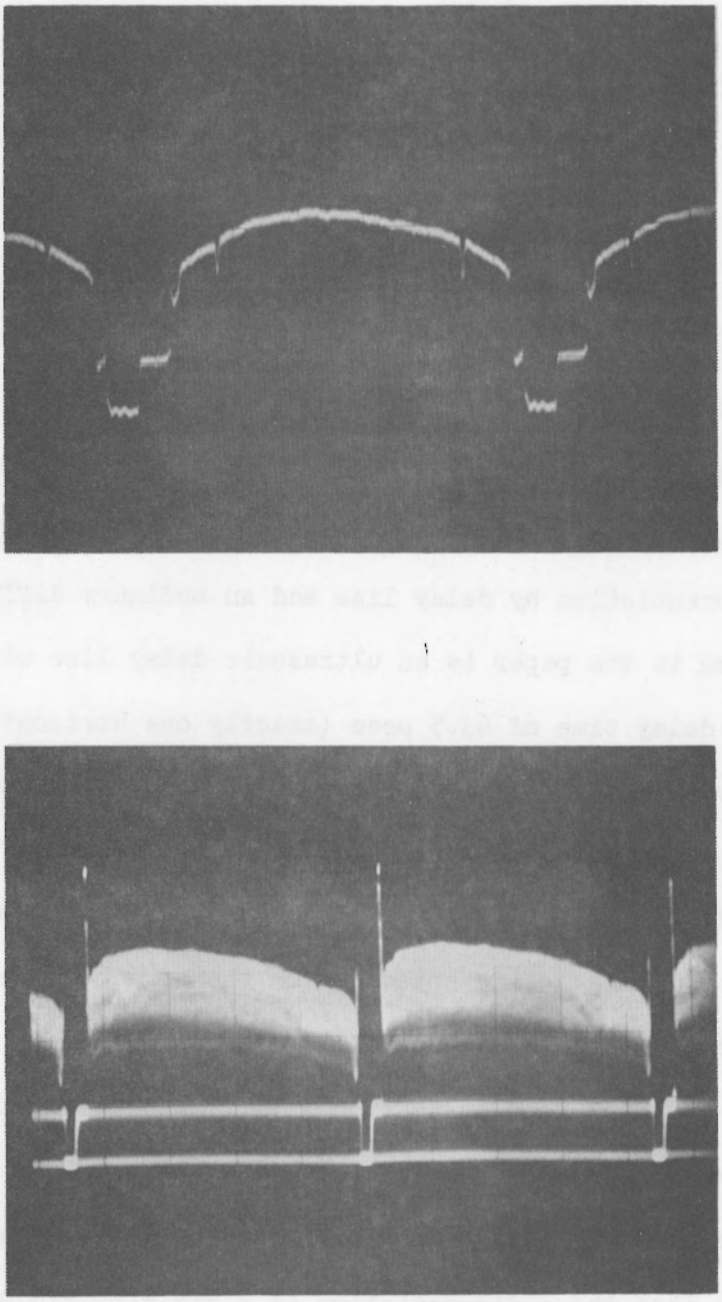


Figure 4. Special Case Video Waveforms

(b) Waveforms of a Black Outline on a White Background

pulses. As might be expected, we see the voltage over a field varies in a very similar manner to that over the line, making any sort of simple threshold detection impractical. We can see that for the black-on-white case, one has to extract usable information from negative-going pulses while for the white-on-black case, one has to extract information from positive-going pulses.

c. The Delay Line Scheme

A paper [8] was located in which an outlining scheme is developed by using the superposition of two differentiations. Ordinary differentiation of the video had been labeled as undesirable because of the fact that all horizontal lines are differentiated out. This paper, however, presents a way of getting around this problem. The scheme involves the superposition of a vertical differentiation by delay line and an ordinary differentiation. The delay line used in the paper is an ultrasonic delay line with a bandwidth of 1.5 MHz and a delay time of 63.5 μsec (exactly one horizontal line). In order to form the "vertical derivative", one must just subtract the delayed video from the real time video. The result of this so-called vertical differentiation is a horizontal line while the result of an ordinary or "horizontal" derivative is a vertical line appearing on the screen. The two, superimposed, form the "total" derivative or the all-direction outline.

As discussed in Section II.A.1, two adjacent (in the time sense) horizontal line waveforms appear on the monitor's CRT face with another line from the other field in between them. A result of the delay being one horizontal line is that the differentiation is a field-by-field differentiation and not a frame-by-frame differentiation. Any horizontal information appearing in the television picture is actually vertically differentiated twice -- once

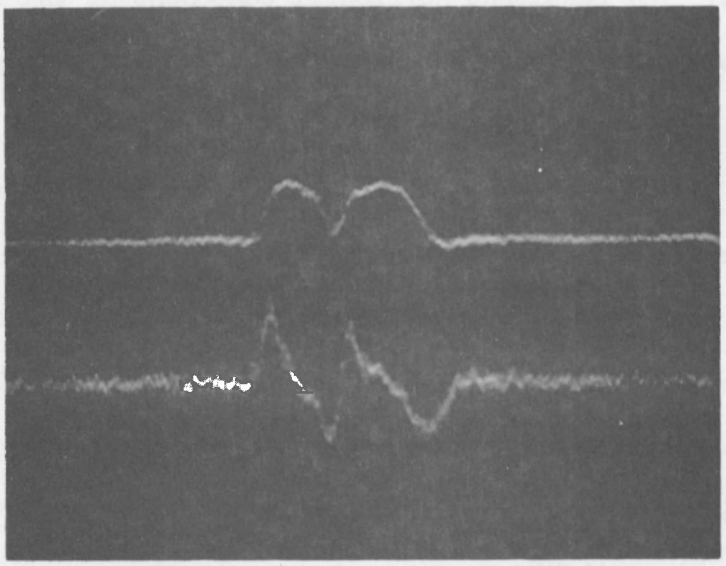
for each field. The resultant horizontal component of the outline is twice as thick as it would be, had it been differentiated frame-by-frame.

d. The Implementation

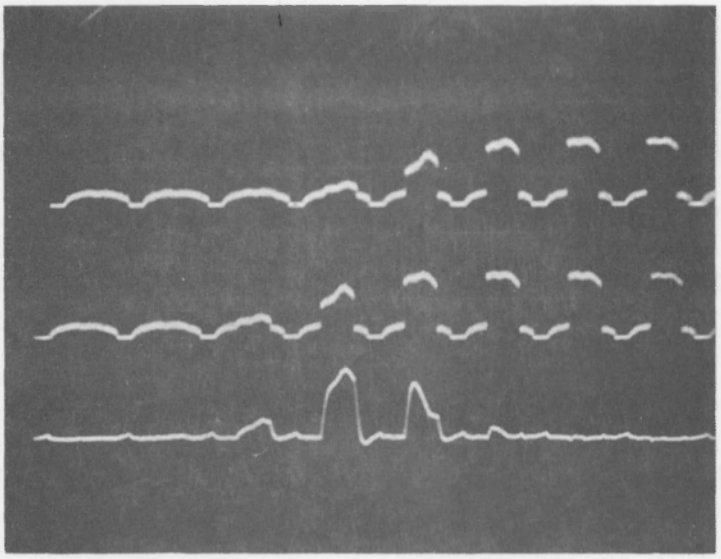
It was not known whether the delay line scheme could be applied to the ATC, because of drift in the disc's speed. The time between HD timing pulses varies, causing the video's line period to change from line to line. A series of experiments were run and the necessary data collected to determine the average line length and standard deviation. The average line length was found to be 63.49184 μsec with a standard deviation of 4.19 nanoseconds. Ultrasonic delay lines available on the market typically specified the delay ±10 nsec. and talks with suppliers indicated that the delay line scheme would work for the ATC - Mark II.

The curvature of the video is no longer a problem due to the fact that this scheme depends only on the difference of two video waveforms with approximately the same shape of curve. Also, this technique avoids any sort of video flattening scheme while preserving the horizontal outline information. The delay line used was purchased from Corning Glass Company. The 3db bandwidth of the Corning delay line is 8 MHz down to 4 Hz. This is actually somewhat better than needed because the 3db bandwidth of the camera is only 7 MHz.

Two different horizontal or ordinary differentiators were built. One, an RC filter differentiator was built experimentally so as to provide a good outline on the monitor when a line drawing is being scanned. The other was built using an 80 nsec delay line. In comparing the two, it is found that they provide essentially the same information. The system has been designed so that either one or the other may be selected. A sample horizontal delay line differentiation is shown in Figure 5(a). Here the top



(a) Sample Horizontal Delay Line Differentiation



(b) Sample Vertical Differentiation

Figure 5. Sample Differentiations

waveform is video and the bottom is its delay line derivative. Figure 5(b) shows a sample vertical derivative. The top waveform is the delayed video, the middle waveform is the real-time video, and the bottom waveform is its "derivative". Photographs of the outlining scheme are discussed in Appendix D.

e. Extension to More General Scenes

The differentiation scheme allows for taking "outlines" of more complex scenes than just line drawings. This may be desirable in order to "color in" a solid object placed in front of the camera. When a general scene is viewed, the Logical Derivative (LD) is extremely scene-content dependent. By this we mean that scenes composed of solid objects require a "double-sided" threshold placed on the derivative, while scenes composed of lines require a "single-sided" threshold. This is illustrated in Figure 6. A "single-sided" threshold detects either the plus or the minus side of the signal while a "double-sided" threshold detects both sides. If the scene viewed is composed exclusively of either solid areas or line drawings, then switches may be set to take the double- or single-sided threshold as desired. For scenes composed of both solid areas and line drawings, a scheme to remove double outlines from the line drawing parts, while not perturbing the solid area outlines, needed to be and was developed.

f. Double Line Correction

Several types of correction were tried. One idea was to OR the double-sided threshold of the first derivative with the double-sided threshold of the second derivative. This scheme is shown in Figure 7(a). Although this seems to be a sound technique theoretically, experiment showed that the double lines remained around the slanty part of the line while disappearing from the more vertical part, as shown in Figure 7(b). The next correction

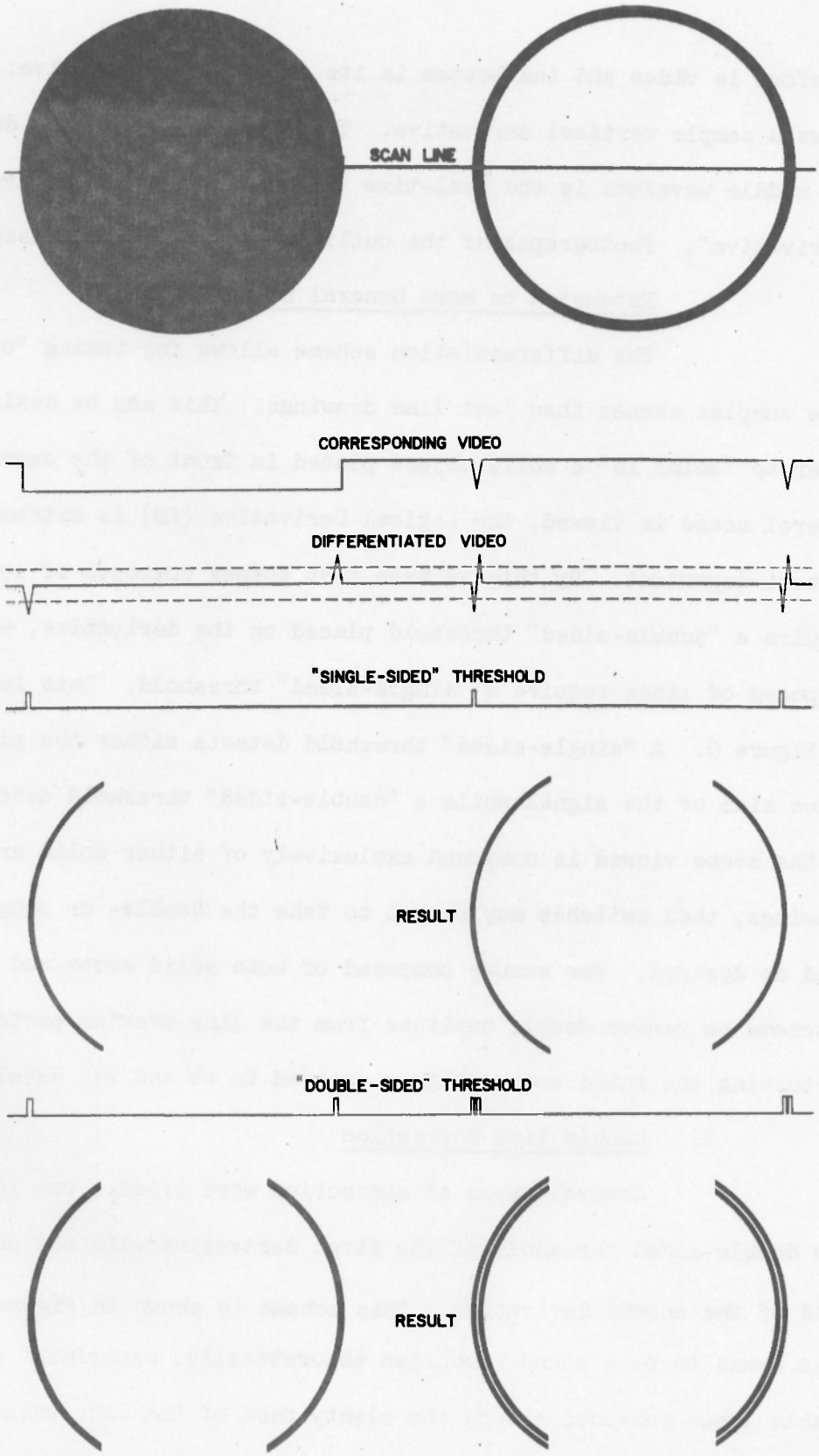
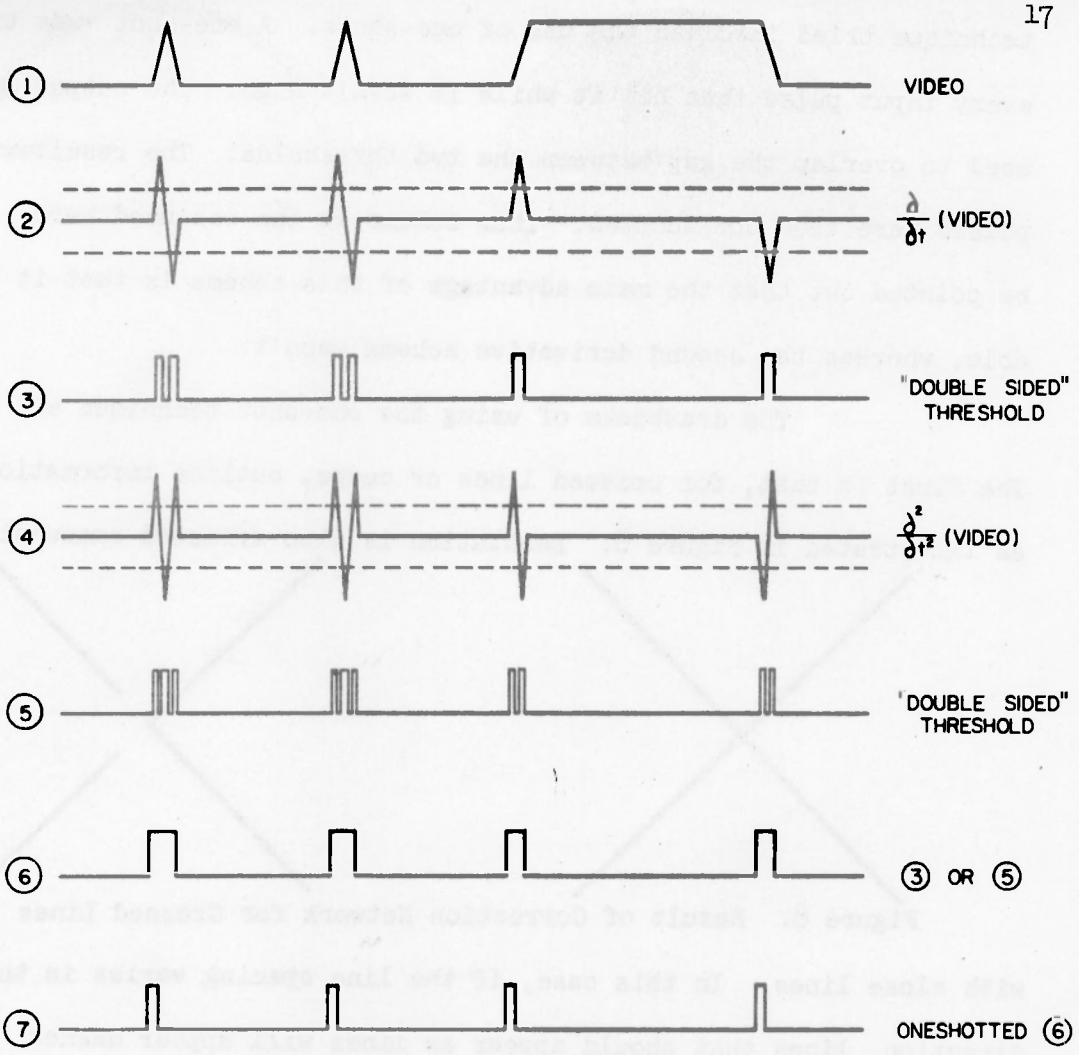


Figure 6. Automatic Outlining (Vertical Components Only)



(a) Sample Waveforms

(b) Result

Figure 7. Second Derivative Scheme

technique tried involved the use of one-shots. A one-shot was triggered with every input pulse that hit it while it wasn't high. The output pulse was used to overlap the gap between the two thresholds. The resultant wide pulses were then one-shotted. This scheme is the one used here. It should be pointed out that the main advantage of this scheme is that it is adjustable, whereas the second derivative scheme wasn't.

The drawbacks of using the one-shot technique are several. The first is that, for crossed lines or cusps, outline information is omitted, as illustrated in Figure 8. Resolution is also affected somewhat for scenes

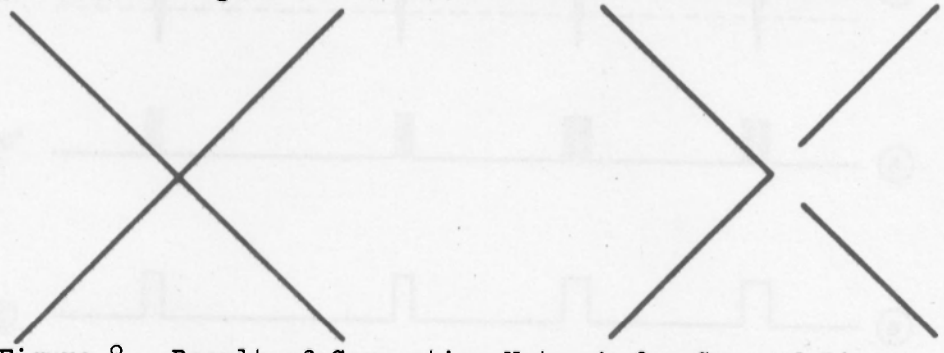


Figure 8. Result of Correction Network for Crossed Lines

with close lines. In this case, if the line spacing varies in the vertical direction, lines that should appear as lines will appear dashed. This occurs if the one-shot cycle is completed between the two thresholds. The one-shot will trigger on the negative threshold instead of the positive, thereby giving the resultant output a zig-zag effect as well as a dashed effect [see Figure 53(b)]. Another drawback is that because the one-shot triggers with any length of input pulse, unnoticeable noise pulses are effectively "multiplied" to become very noticeable. Various possibilities exist for forming the vertical derivative correction. None were tried, however, because of monetary considerations. The vertical derivative is left uncorrected here. Appendix D discusses a photograph of a corrected outline which illustrates these drawbacks.

2. The Vertical Stripe Problem

In the ATC, the COLOR signal is chopped at 3 MHz in one phase during an odd field and 180° out of the odd-field phase during an even field. In the ATC - Mark I, the Disc Read Amplifiers were operated in the Class B mode so that the outputs took the form of half wave rectified sine waves. The superposition of the two fields then produced areas of color with vertical stripes in them corresponding to the nulls or peaks of virtual full wave rectified sine waves. It was decided to use a demodulator to detect when a sine wave is being read. The Disc Read Amplifiers were redesigned to operate in the Class A mode to provide the demodulators with a suitable signal. The disc speed variations mentioned before and phasing problems require that the reference or carrier frequency be derived from the signal itself. The demodulator used is amplitude sensitive so as to provide for shades of gray capability.

3. Shades of Gray Capability

The work leading to Mark I of the ATC was concerned primarily with the development of a coloring algorithm, and so, shades of gray capability was not included. It was felt that shades of gray capability would sizably increase the scope of the machine and was, therefore, included as a goal in the ATC - Mark II.

a. The Disc

It was not known if the disc was shades of gray compatible. To prove that it was, a ramp generator was synchronized to the HD of the disc, and the ramp was then gated into the write input of a disc channel. The output of that channel's Disc Read Amplifier was then viewed on an oscilloscope and a photograph of this scope trace is shown in Figure 9. This experiment proved that the disc was shades of gray compatible. The range of input signals for outputs in the linear range is from about 0.7 volt to about 1.0 volt.

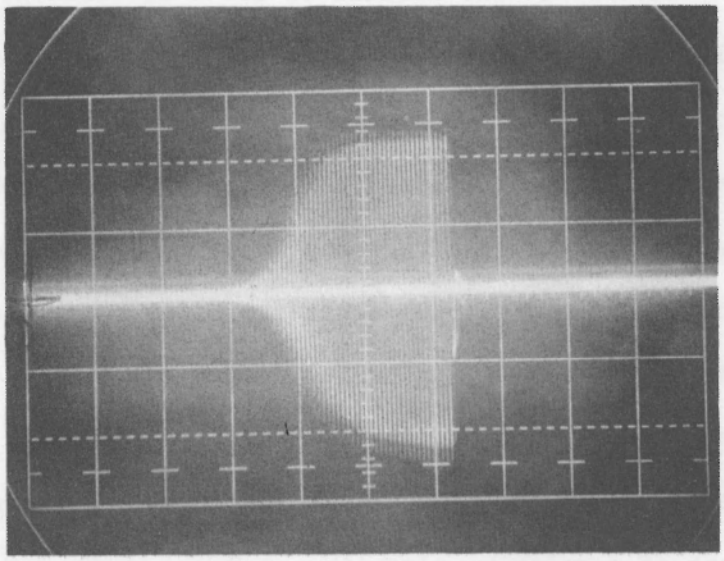


Figure 9. Disc Response to a Ramp

Sweep ~ 1 Horizontal Line

b. The Implementation

The implementation is very straightforward. Control of shading is by means of three potentiometers located on the Control Panel. The operator positions the potentiometers according to a "PREVIEW COLOR" area viewed on the CRT face. The amplitude of the COLOR signal is then clipped to a value corresponding to the potentiometer positions and channeled into the disc's write inputs. A chopper in the disc unit chops this signal before it is written on the disc's surface.

III. THE CIRCUITRY FOR THE ATC - MARK II

With a few exceptions, the circuitry described here does not appear in Reference [1], "A Tricolor Cartograph". The schematic drawing of the coloring logic is included in order to give a better insight into the overall design of the machine. Any modified circuitry is included here, but circuitry that hasn't been changed remains as described in [1].

A. Drawing Conventions

Before embarking on the circuitry descriptions, it will be helpful to the reader to list the drawing conventions. First, the great majority of the circuitry described here is assembled on 22 pin printed circuit (PC) cards. Input/output pins on these cards are lettered on the component side of the board and numbered on the noncomponent side as follows:

Component side

A B C D E F H J K L M N P R S T U V W X Y Z

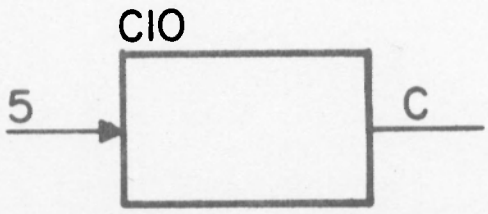
[A through Z with G, I, O and Q omitted]

Noncomponent side

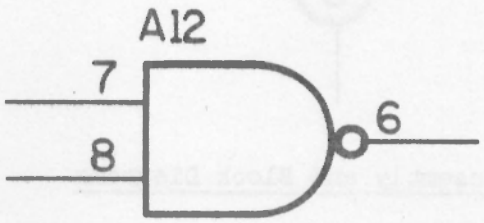
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22

[1 through 22]

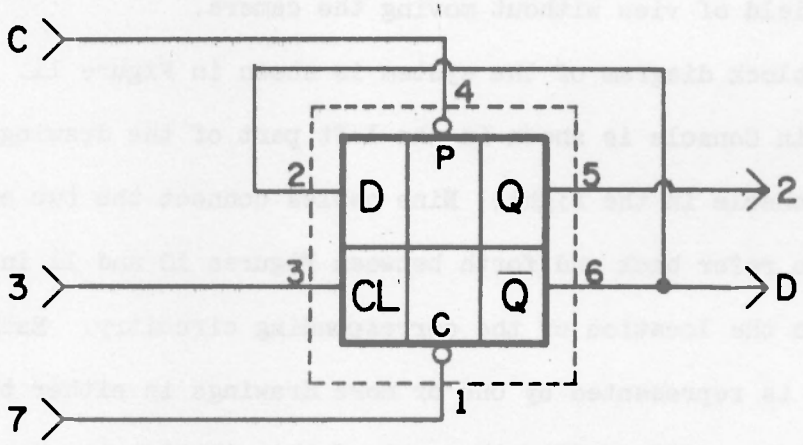
In the card rack, there are three rows of cards, each row holding 28 cards. The top row is labelled A, the second B, and the third C. The Ultrasonic Delay Line is mounted horizontally below card rack C and is labelled card D1. The block diagram of the card shown below means that the input is pin 5, the output is pin C, and the card is the tenth card in the bottom row.



A generalized NAND is labelled in much the same way, as is shown below. Here the inputs are PC card pins 7 and 8, the output is pin 6, and the card is the twelfth card in the top row.



In this case, it is important not to confuse the card pin numbers with the integrated circuit (IC) pin numbers. The detailed card drawings label card pins as shown in the drawing below.



In this drawing, pins C, 3, and 7 represent PC card inputs, while 2 and D represent PC card outputs. The IC pin numbers are the numbers located just outside of the dotted square. All common points and power supply voltages are indicated by square boxes such as shown below.

Original printed circuit layouts are labelled with the PC card number which always starts with 1469, the contract number. A logical zero is -5 volts, and a logical 1 is ground. These are denoted as shown below.

B. Mechanical Assembly and Block Diagrams

The mechanical assembly of the ATC - Mark II is shown in Figure 10. The light pen, the shading potentiometers, and the control switches allow for operator interaction. A bundle of cables connects the Display Console to the Main Console. An F1.5, 22.5 to 90 mm zoom lens on the camera allows for changing the field of view without moving the camera.

The block diagram of the system is shown in Figure 11. The block diagram of the Main Console is shown in the left part of the drawing and that of the Display Console in the right. Nine cables connect the two consoles. It is helpful to refer back and forth between Figures 10 and 11 in order to relate a block to the location of the corresponding circuitry. Each block in Figure 11 is represented by one or more drawings in either the Kubitz thesis [1] or in this one. In reading the rest of this thesis, the reader should keep this block diagram in mind.

1. The Sync Converter Delay Circuit

The camera, located on top of the Display Console, requires sine wave synchrhonization. A commerically available sync converter was purchased to make the HD - sine wave conversion. For some reason, however, the camera and the monitor didn't want to start scanning at the same time, so that the camera's blanking appeared in the middle of the screen. The circuit shown in

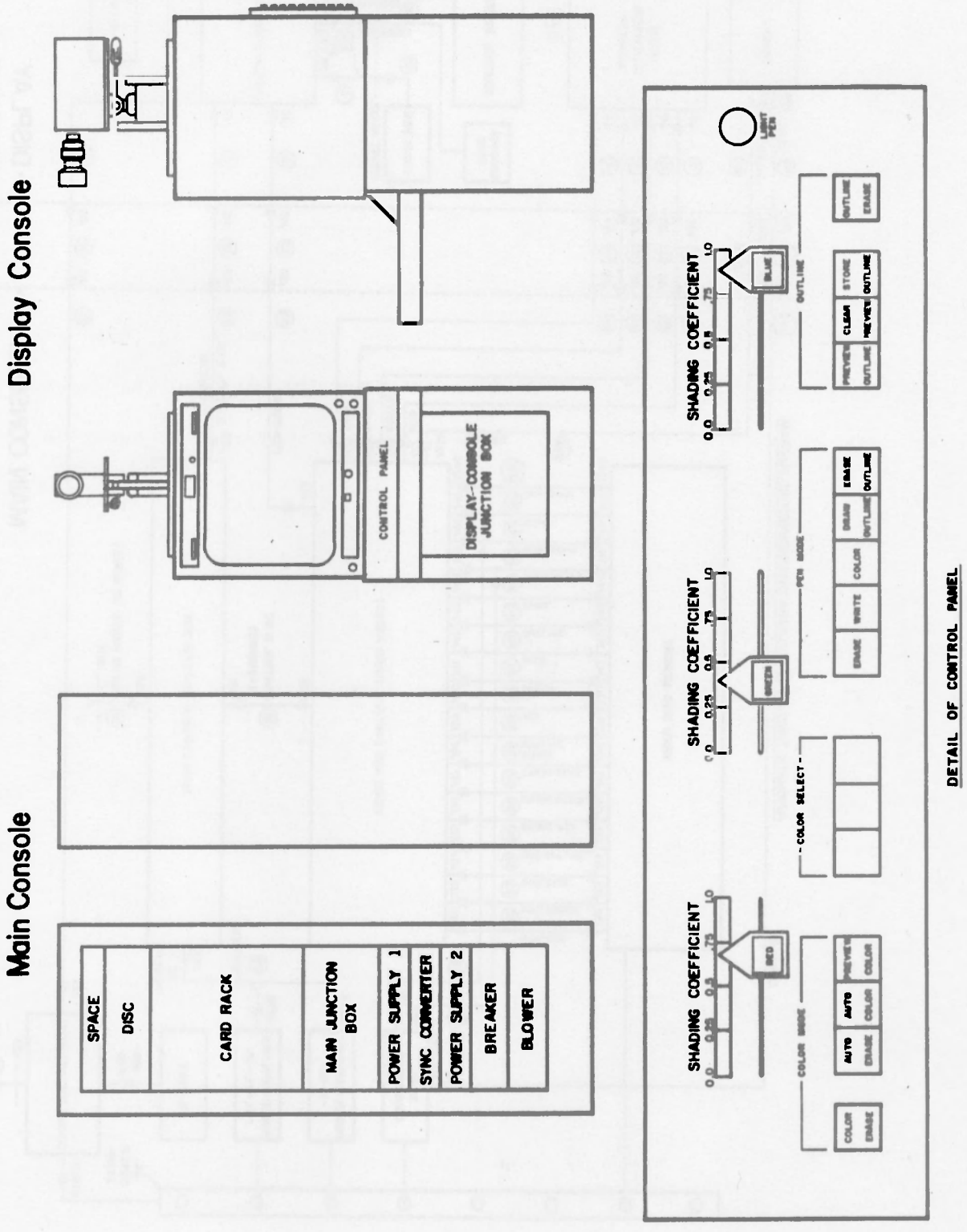


Figure 10. Mechanical Assembly

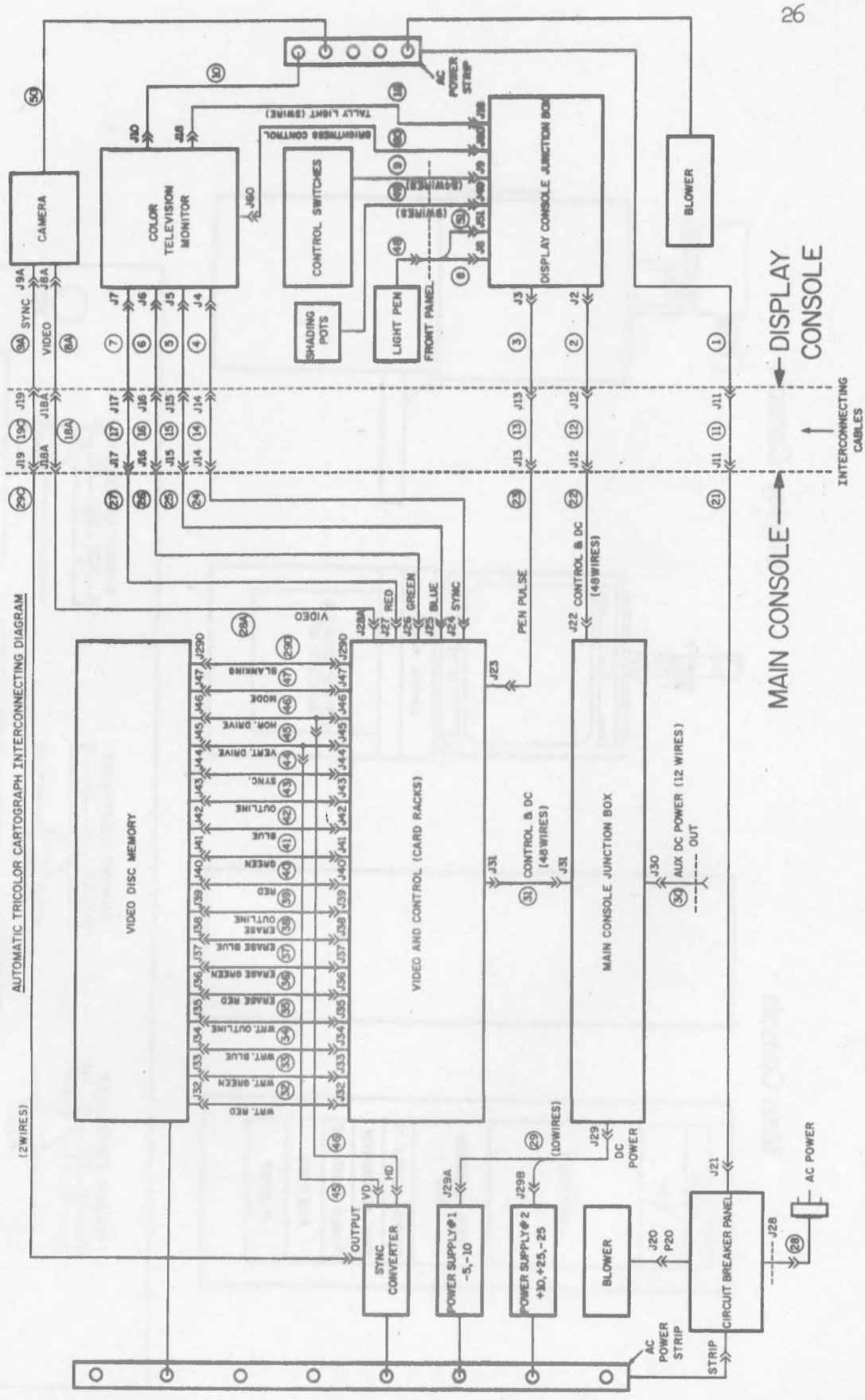


Figure 11. System Block Diagram

Figure 12 was built, using the sync converter power supply, to delay HD by a time determined by the setting of potentiometer P1. Typical waveforms are shown below the circuit.

2. The Control Panel and Display Console Junction Box

The operator interacts with the system with the light pen and by setting the switches and potentiometers shown in Figure 10. The mechanical assembly of the Control Switches is shown in Figure 13. Mechanical interlocks are used in some cases to make the switches mutually exclusive. Figure 14 shows the schematic of the Control Panel. The "AUTO ERASE", "AUTO COLOR", "PREVIEW COLOR", "PREVIEW OUTLINE", "CLEAR OUTLINE" and "STORE OUTLINE" switches are new. The "AUTO ERASE", "AUTO COLOR" and "PREVIEW COLOR" switches are mutually exclusive, and allow the operator to automatically erase or color the inside of an outline or to adjust the shading potentiometers for a desired color (preview the color). The "PREVIEW OUTLINE", "CLEAR OUTLINE" and "STORE OUTLINE" switches are mutually exclusive except that the "CLEAR OUTLINE" and "STORE OUTLINE" switches do not stay in when pushed. The "PREVIEW OUTLINE" switch allows the operator to adjust the camera while looking at the outline on the CRT. The "STORE OUTLINE" switch pops the "PREVIEW OUTLINE" switch out and records one frame of outline information on the disc. The "CLEAR OUTLINE" button pops out the "PREVIEW OUTLINE" button without recording anything.

In each case, the switch signal comes from Switch A. Switch B is used to light the light bulbs inside of the button. The switch and shading potentiometer signals then go to the Display Console Junction Box, shown in Figure 15, where they are processed before routing to the Main Console.

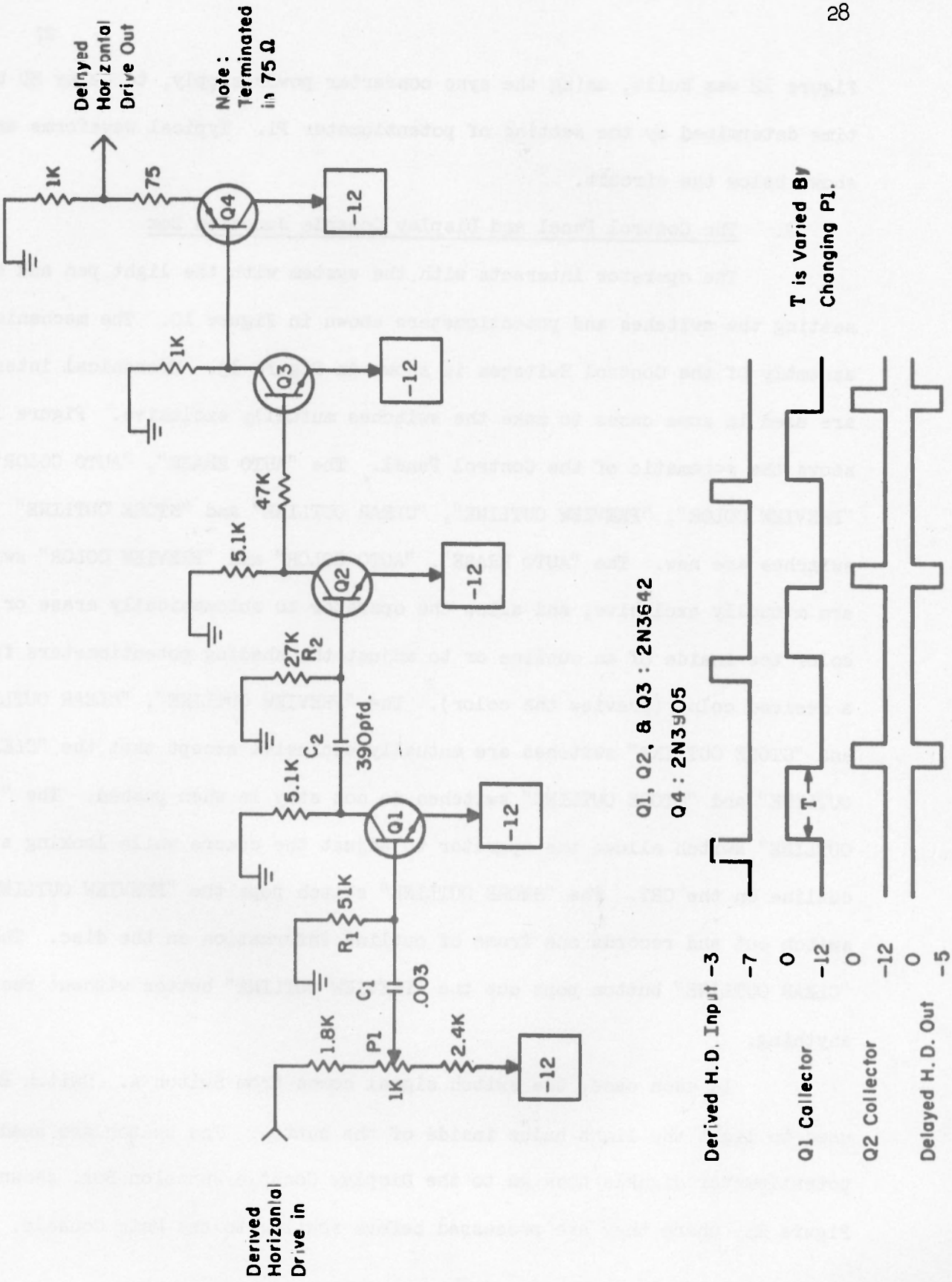


Figure 12. Sync Converter Delay Circuit

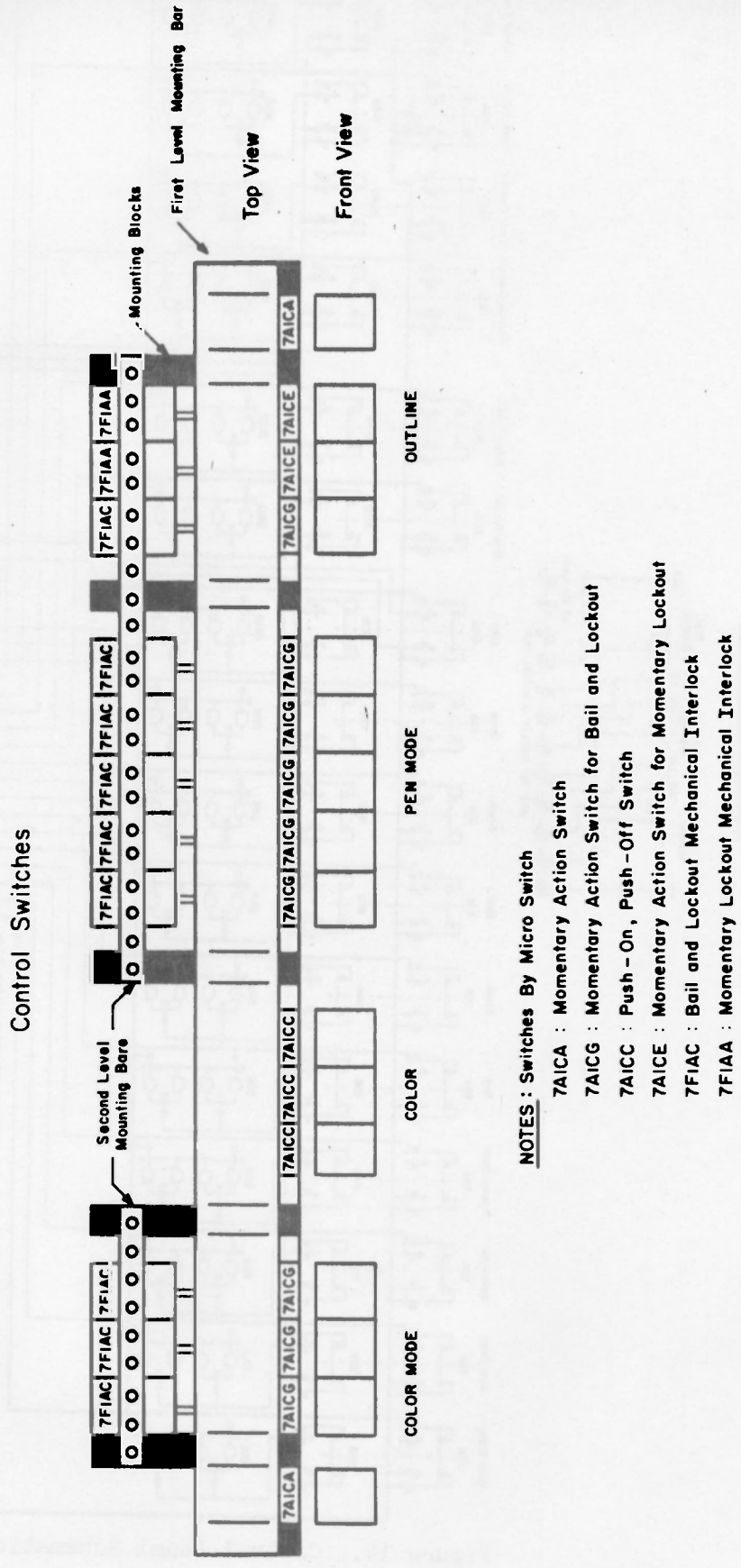


Figure 13. Mechanical Assembly of Control Switches

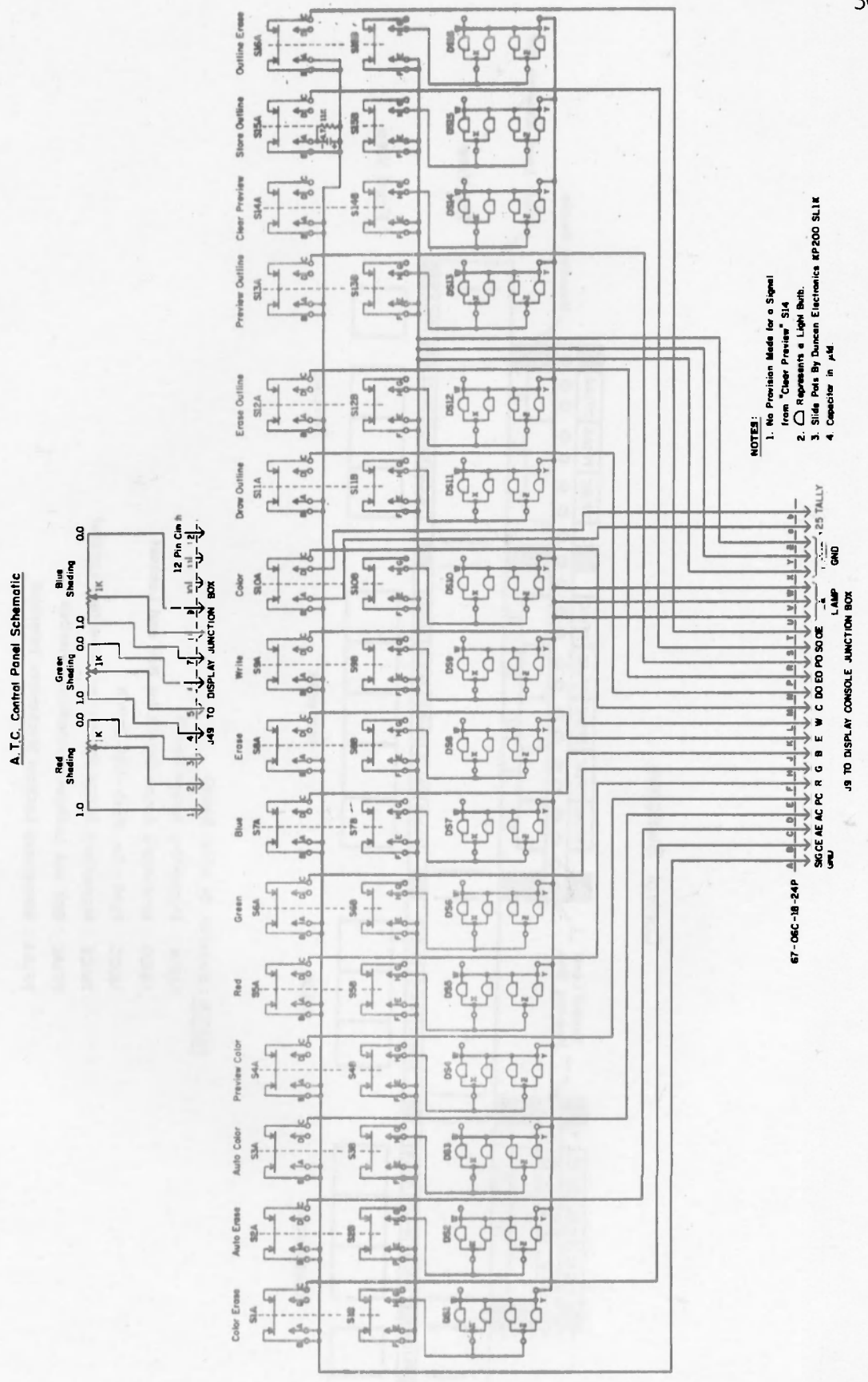


Figure 14. Control Panel Schematic

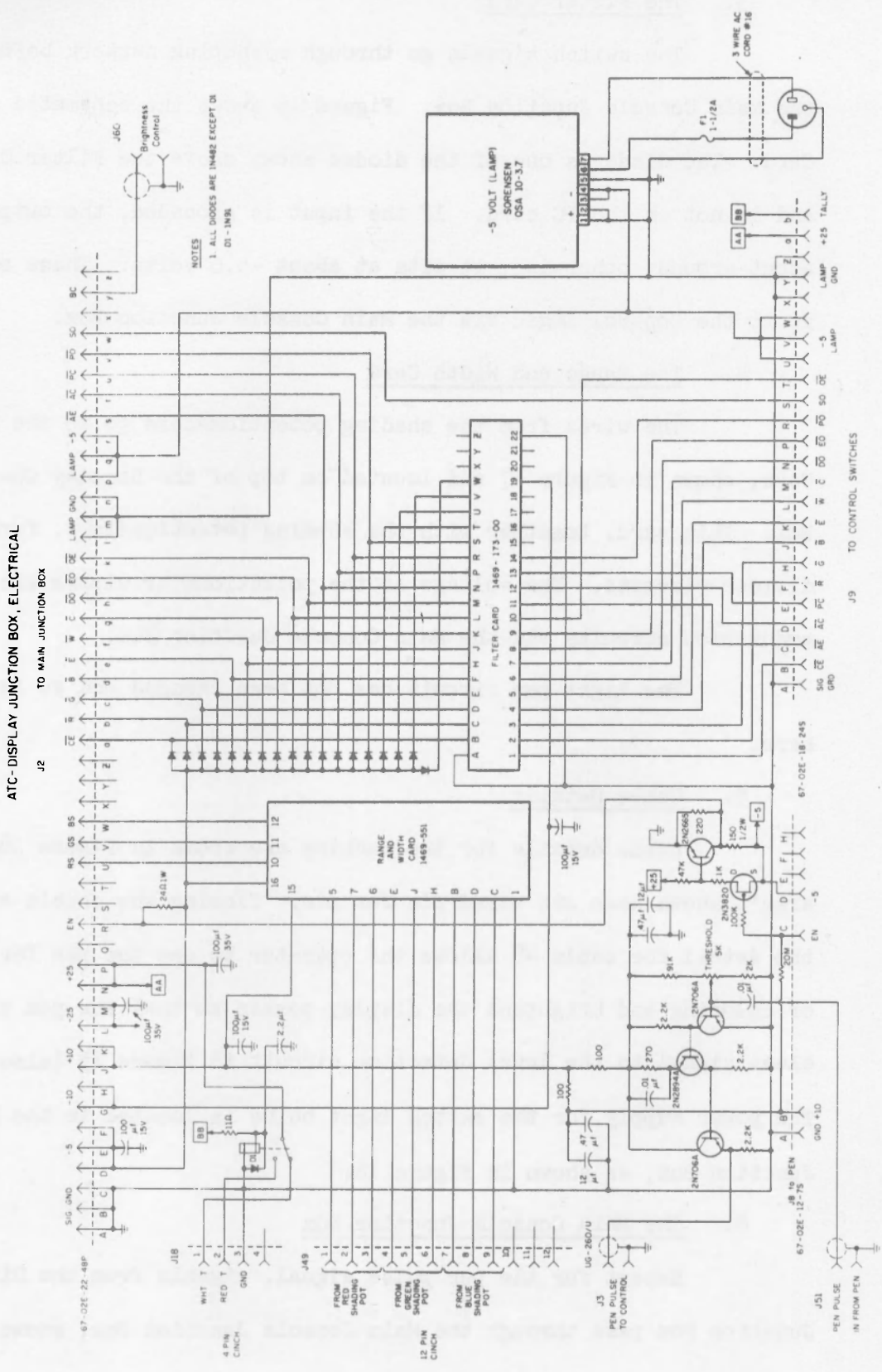


Figure 15. Display Console Junction Box

3. The Filter Card

The switch signals go through a shaping network before going on to the Main Console Junction Box. Figure 16 shows the schematic of the Filter Card. The diode is one of the diodes shown above the Filter Card in Figure 15 and is not on the PC card. If the input is grounded, the output sits at about ground; otherwise, it sits at about -5.6 volts. These shaped signals go to the Control Logic via the Main Console Junction Box.

4. The Range and Width Card

The wires from the shading potentiometers go to the Range and Width Card, shown in Figure 17 and located on top of the Display Console Junction Box. This card, together with the shading potentiometers, forms voltage divider circuits. The voltage at the potentiometer wipers are sent to the modulation circuits via the Main Console Junction Box.

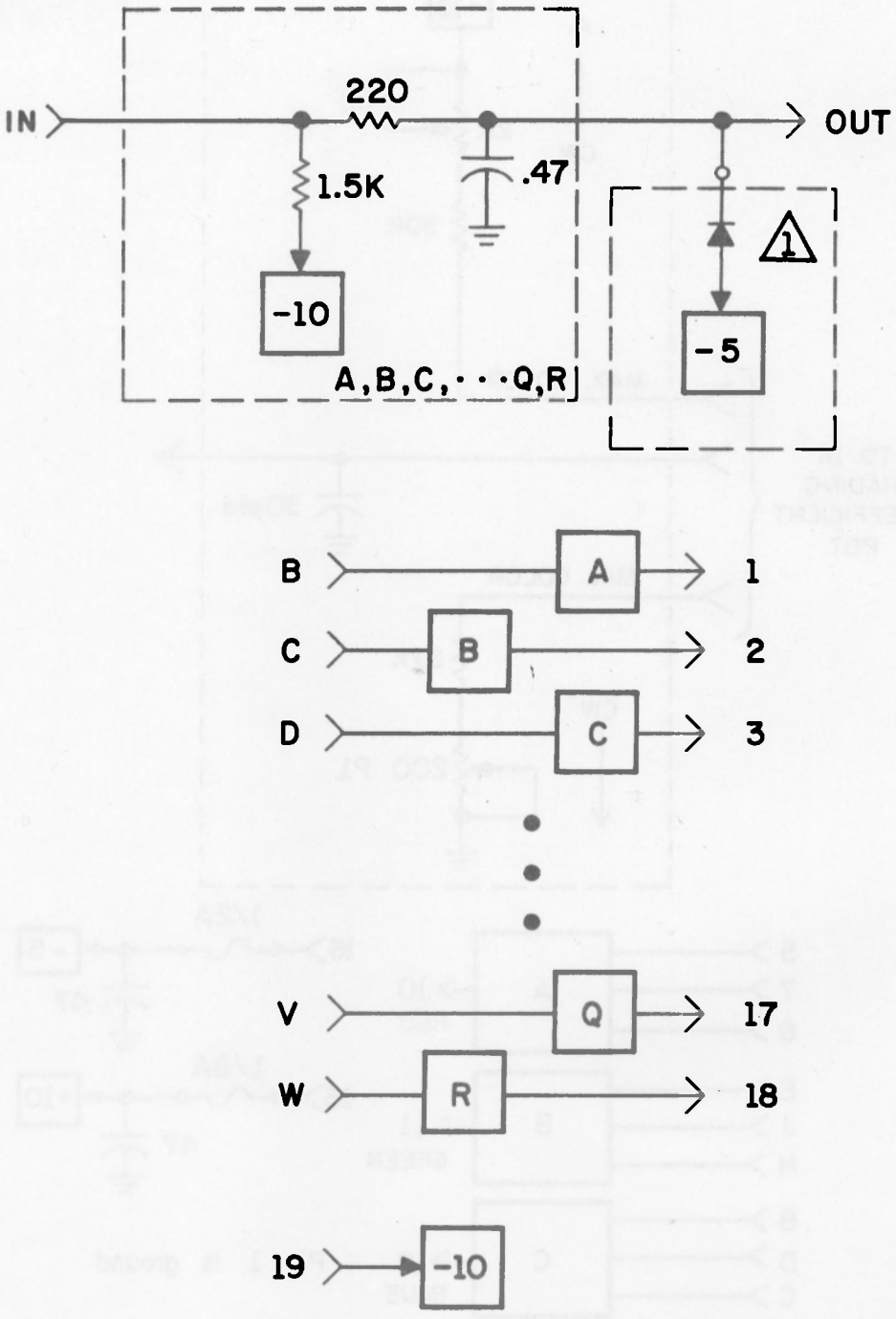
The light pen circuit has not been changed and so is not included here.

5. Cable Details

Cable details for the machine are shown in Figure 18. Cables that aren't shown here are wired pin for pin. Closing the enable switch shown in the detail for cable 48 allows the operator to use the pen for drawing outlines or coloring and brightens the display screen so that the pen can provide a clean signal to the level detection circuit in Figure 15 (also see Figure 11). The power supply for the switch light bulbs is located in the Display Console Junction Box, as shown in Figure 15.

6. The Main Console Junction Box

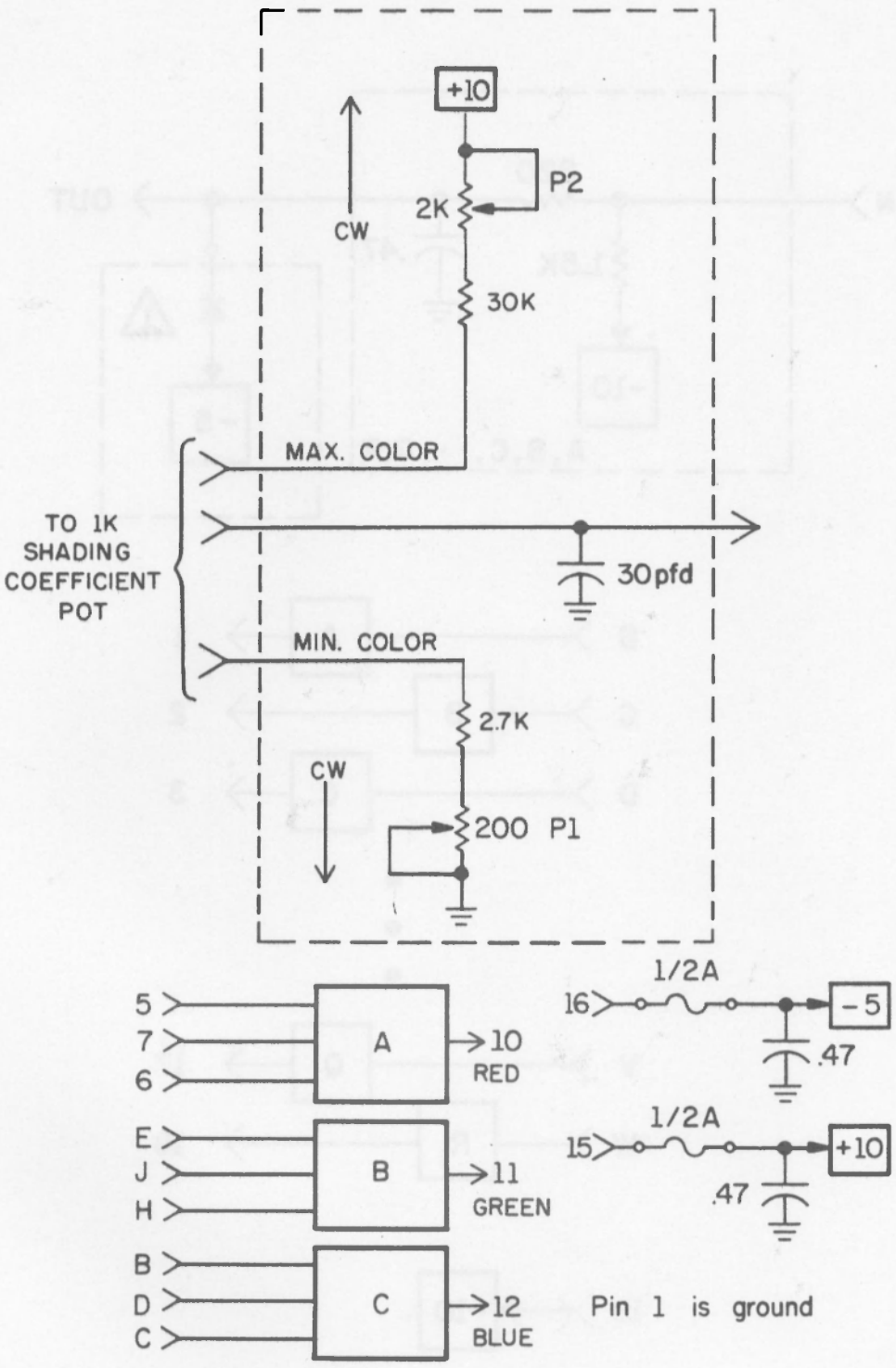
Except for the pen pulse signal, signals from the Display Console Junction Box pass through the Main Console Junction Box, shown in Figure 19,



NOTES: 1 DIODE NOT PART OF SWITCH FILTER CARD. SHOWN TO ILLUSTRATE COMPLETE CIRCUIT.

2. A, 22 ARE GROUND

Figure 16. Switch Filter Card (1469-173)



NOTE:
OUTPUT VOLTAGE RANGE .770V to 1.010V

Figure 17. Range and Width Card (1469-551)

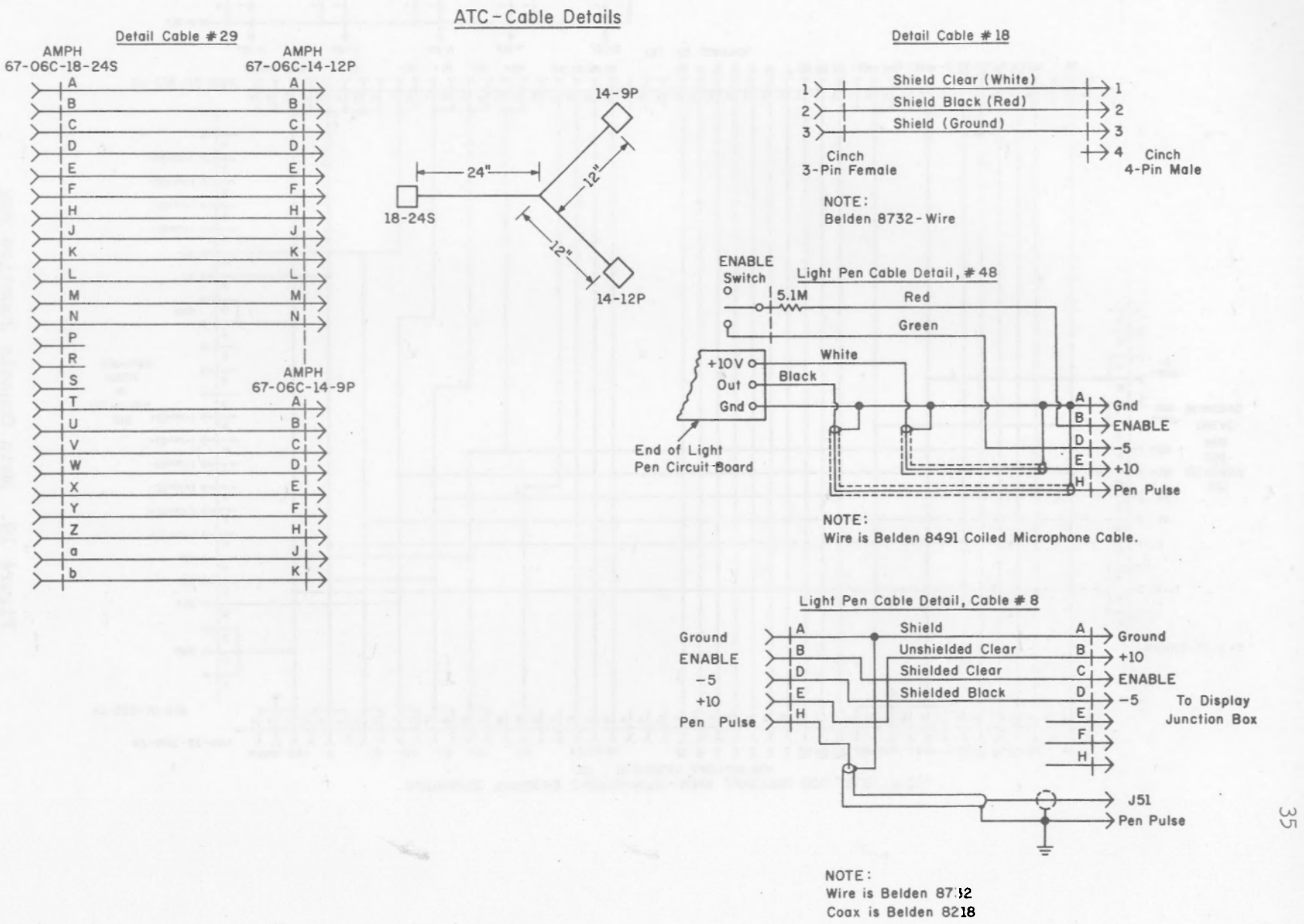


Figure 18. Cable Details

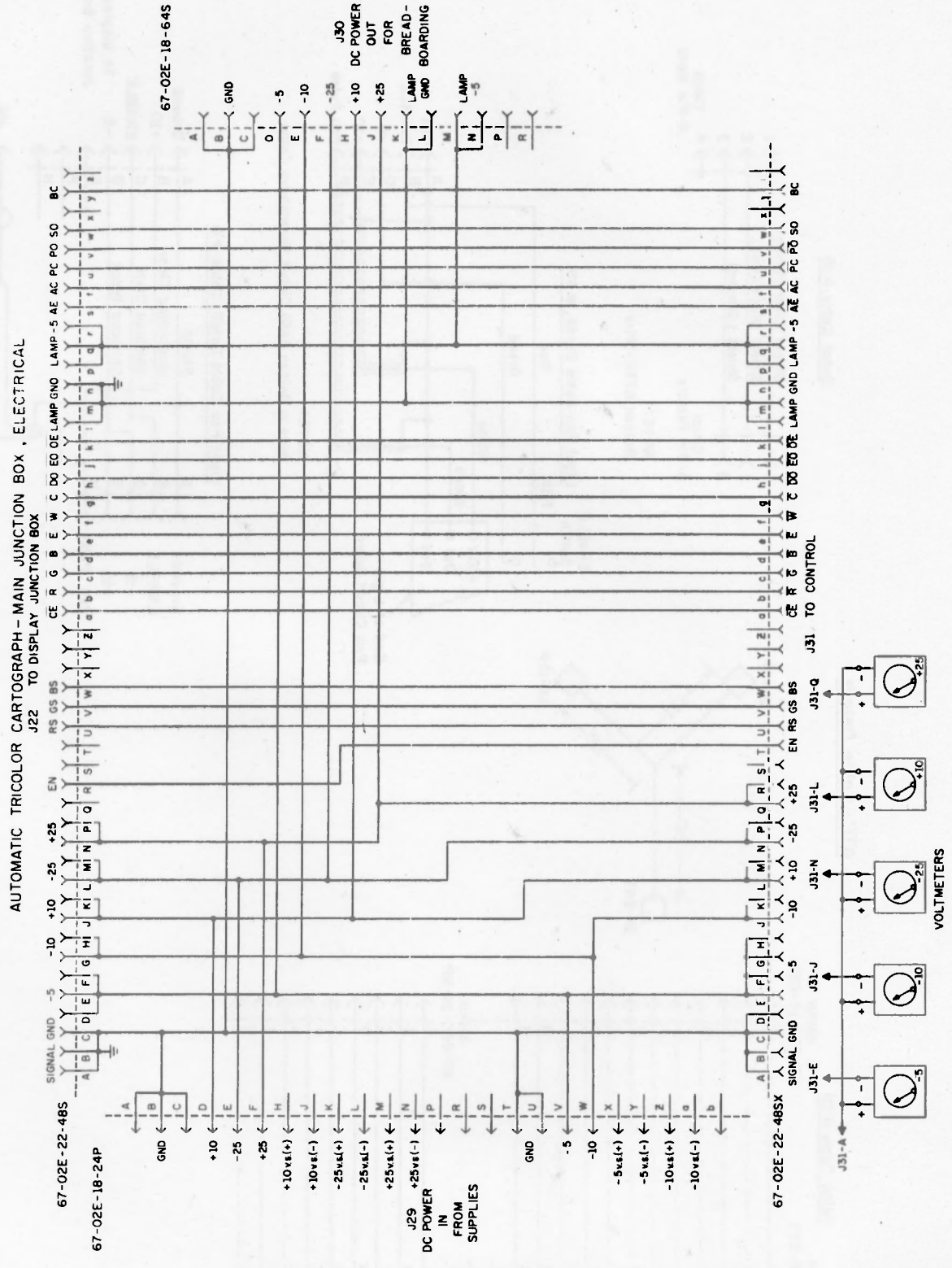


Figure 19. Main Console Junction Box

before proceeding on to the card racks. DC power enters the Main Console Junction Box where it is routed to the Display Console Junction Box and the card racks.

7. The Card Racks (Video and Control)

The block in the System Block Diagram, Figure 11, labeled Video and Control (card racks) has in turn been broken into three other block diagrams. The division has been done primarily by function. The central drawing, shown in Figure 20, is the "ATC Video and Control Logic" drawing. Appended to it are two other functional block diagrams, the "ATC Coloring Logic," and the "ATC Outlining Circuitry". These drawings are shown in Figures 21 and 22, respectively. Wiring cross references between drawings are indicated with circled numbers. The signals to and from the disc are routed through the coaxial connectors, and the control signals and DC power from the Main Console Junction Box are shown entering through connector J31 in Figure 20. The Coloring Logic has not been changed in the ATC - Mark II. For a complete explanation of this drawing, see Reference [1]. It is included here for easy reference. A more complete discussion of the "ATC Video and Control Logic" drawing will be given with the discussion of the shading circuitry.

C. The Outlining Circuitry

The Outlining Circuitry described below is a new feature in the ATC - Mark II. The block diagram for the Outlining Circuitry is given in Figure 22. Inputs are Logical Vertical Drive (LVD), Logical Horizontal Drive (LHD), the video, Preview Outline (PO) and Store Outline (SO). PO and SO are derived from switch positions on the front panel, the video is from the camera, and LHD and LVD are timing pulses from the disc. Outputs are an inverted gated LOGICAL DERIVATIVE (LD) signal $(\overline{LD})\cdot(GO)$, a signal representing a Preview

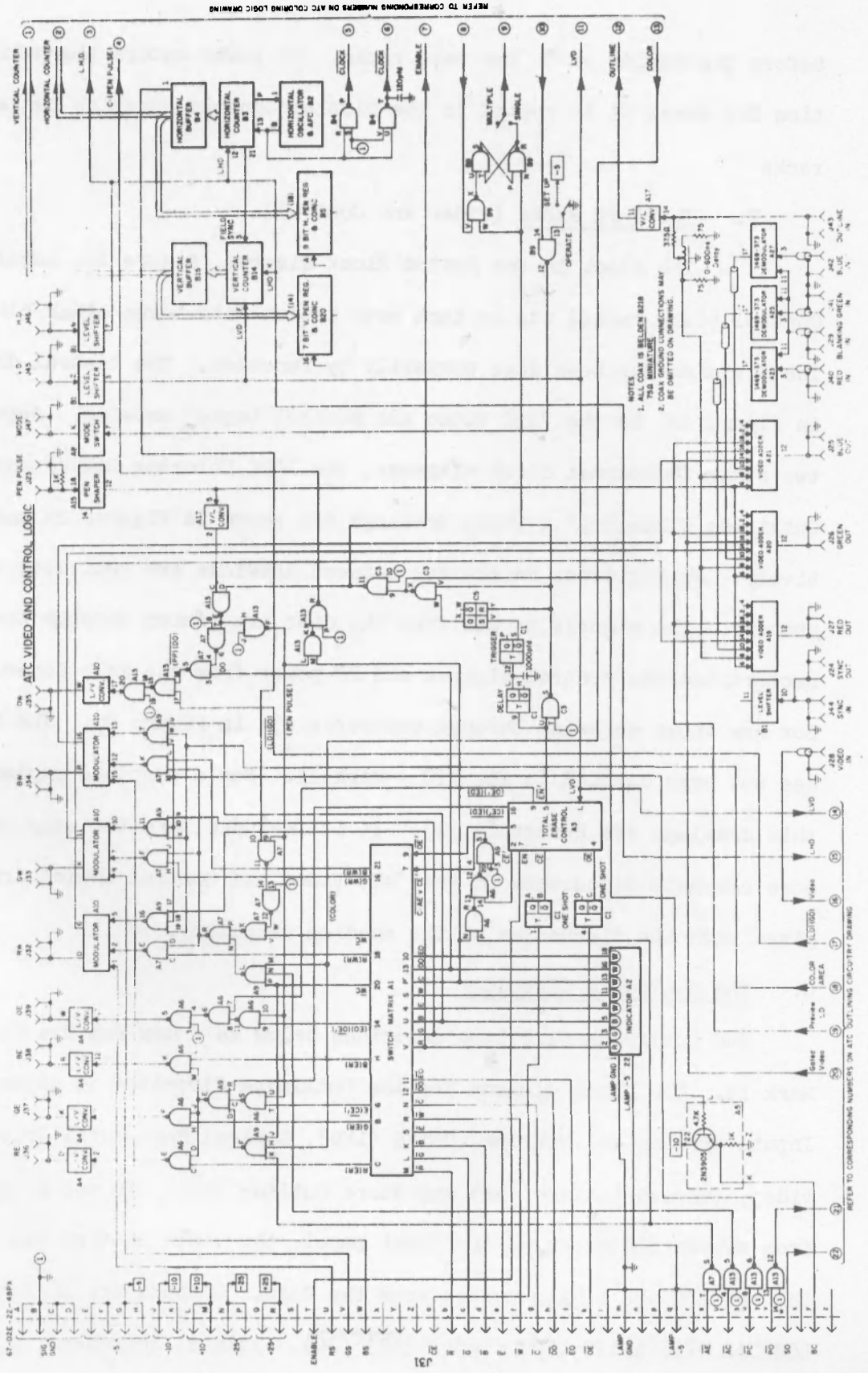


Figure 20. Video and Control Logic

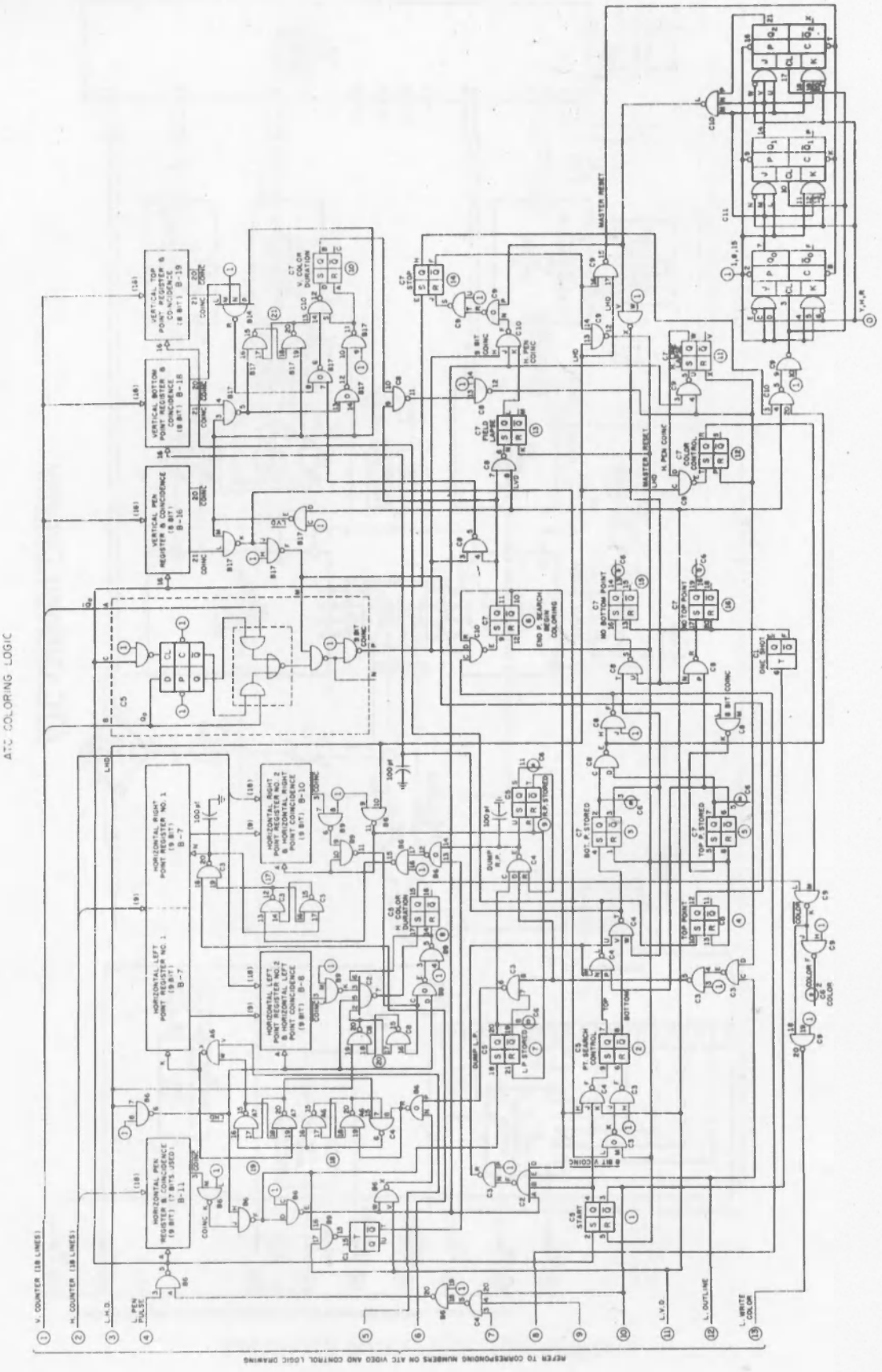


Figure 21. Coloring Logic

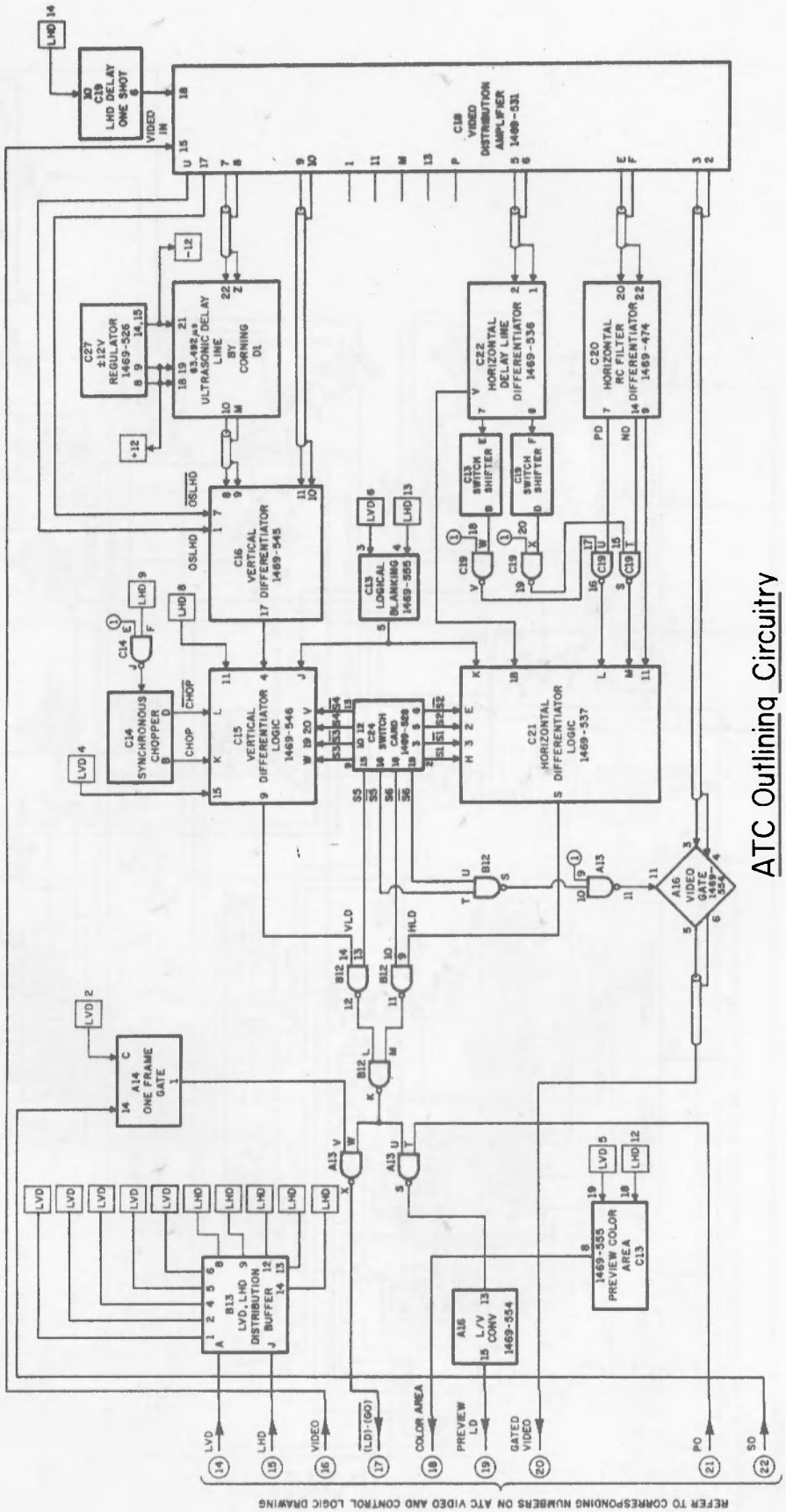


Figure 22. Outlining Circuitry

Color Area, a signal to preview the LD (the outline information) and a gated video signal. To see where the inputs and outputs come from or go to, the reader should refer to the corresponding numbers in Figure 20.

The video signal goes to a Video Distribution Amplifier (VDA) which has provision for ten outputs. LHD is used to clamp the video to a reference level. One output from the VDA goes to the Ultrasonic Delay Line, the output of which goes to the Vertical Differentiator along with another VDA output. Clamping pulses are also used in the Vertical Differentiator. Other VDA outputs go to the horizontal differentiators and the Video Gate.

The output of the Vertical Differentiator goes to the Vertical Differentiator Logic along with chopping signals keyed to LHD, blanking keyed to LHD and LVD (LB) and selection signals from the Switch Card. The outputs of the horizontal differentiators go to the Horizontal Differentiator Logic along with Logical Blanking (LB) and selection signals from the Switch Card. Level shifters are used to shift switch signals coming from the Horizontal Delay Line Differentiator to logic levels suitable for selecting the RC Filter Differentiator outputs. The output of the Vertical Differentiator Logic is a Vertical Logical Derivative (VLD) and of the Horizontal Differentiator Logic is the Horizontal Logical Derivative (HLD). VLD and HLD are ORed together selectively using Switch Card signals to form the LD. Table 1 gives the action for Switch Card switch positions and Table 2 gives the action for 3-position switch positions.

If both HLD and VLD are disabled from forming the LD, the video is gated onto the screen. Otherwise, the LD can be either previewed (by pushing the PO button) or gated onto the disc (by pushing the SO button). The SO signal goes to a one-frame gate where the gate outline (GO) signal is

Switch Position	HLD
0 0	RC Filter Differentiator (One-Shotted Output)
0 1	Delay Line Differentiator (Not One-Shotted)
1 0	RC Filter Differentiator (Not One-Shotted) Leading Edge Only
1 1	Delay Line Differentiator (One-Shotted) and Double Line Corrected

Switch Position	VLD
0 0	Vertical Differentiator (Not Chopped)
0 1	Vertical Differentiator Even/Odd Field Chopped
1 0	Vertical Differentiator Odd/Even Field Chopped
1 1	Vertical Differentiator Chopped

Switch Position	LD/Video
0 0	Gated Video (Camera)
0 1	HLD
1 0	VLD
1 1	HLD v VLD

Table 1. The Switch Card Positions

Vertical Differentiator
Switch on C16

Position	ACTION
Up	Trailing Edge (Single-Sided Threshold)
Center	Both Edges (Double-Sided Threshold)
Down	Leading Edge (Single-Sided Threshold)

Horizontal Differentiator
Switch on C22

Position	ACTION
Up	Trailing Edge (Single-Sided Threshold)
Center	Both Edges (Double-Sided Threshold)
Down	Leading Edge (Single-Sided Threshold)

Table 2. Three-Position Switch Positions

formed from LVD. (LD)·(GO) is then ORed with any light pen signals before proceeding to the disc. A block that is not part of the Outlining Circuitry is also included in this block diagram. This is the block labelled Preview Color Area. The circuit details and appropriate comments, where needed, are given below. The number after the card name is the number assigned to the printed circuit card.

1. The Delay One-Shot and Switch Shifters

The circuit diagrams for the Delay One-Shot and Switch Shifters are shown in Figure 23. The one-shot is used to generate a delay signal from LHD. This is necessary because there is a slight delay between the LHD pulse and the video's sync interval. A delayed HD pulse is formed from this delay signal to clamp the video in the Video Distribution Amplifier (VDA).

The Switch Shifters are used in connection with the horizontal differentiation circuits to convert a zero volt to +5 volt switching signal to a zero volt to -5 volt switch signal.

2. The Video Distribution Amplifier (VDA) (1469-531)

The VDA is used to:

(1) clamp the video at a DC level,

(2) clip the sync from the video,

and (3) provide up to 10 isolated outputs.

The circuit diagram of the VDA is shown in Figure 24. A synchronous clamp [9], synchronized to shortened LHD pulses (OSLHD), clamps the video at a clamp/clip level set by P2. The one-shot provides clamp pulses that are slightly narrower than the camera's horizontal sync. More detailed discussions of the synchronous clamp circuit are found in [9] and [4].

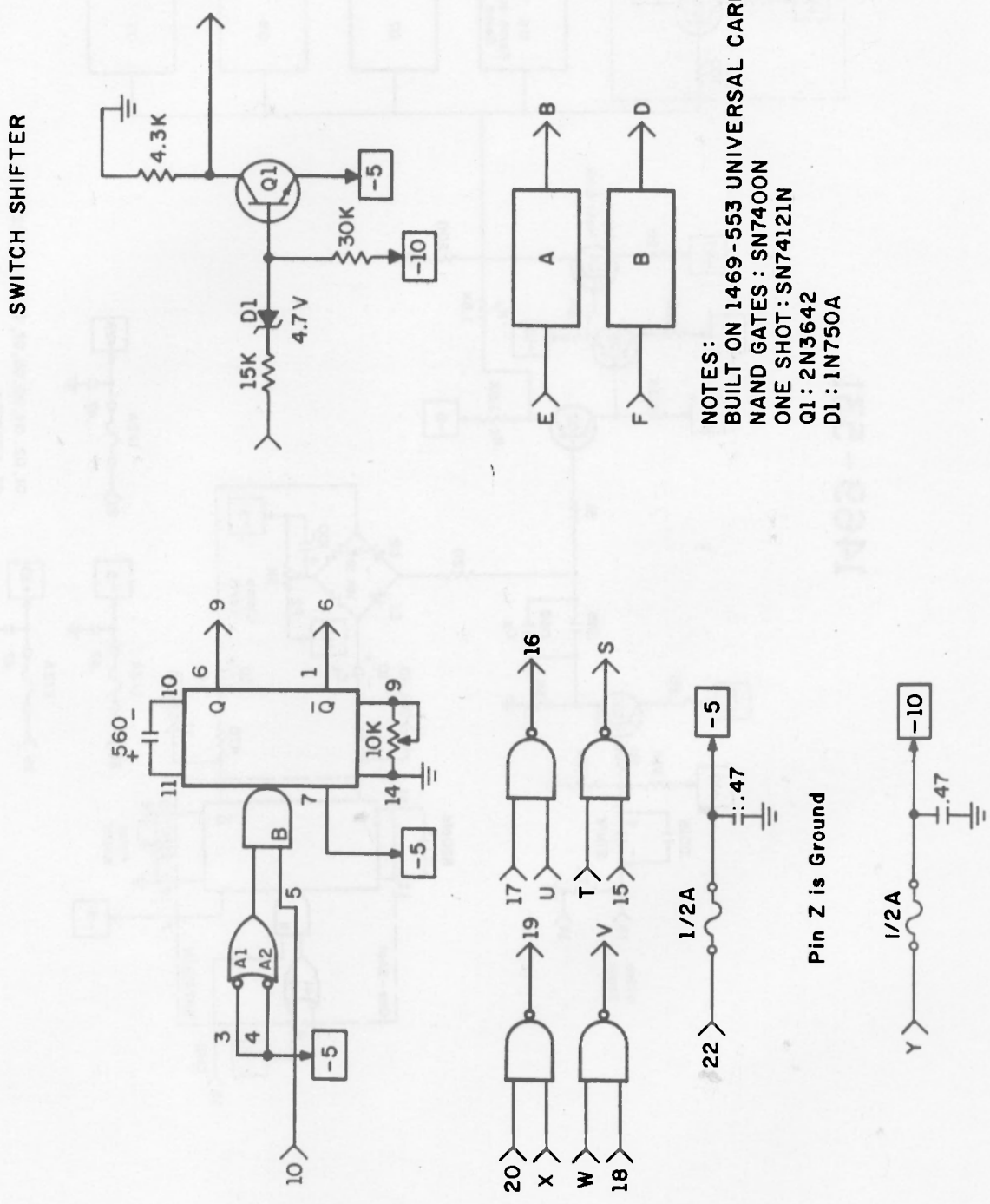


Figure 23. Delay One-Shot and Switch Shifters

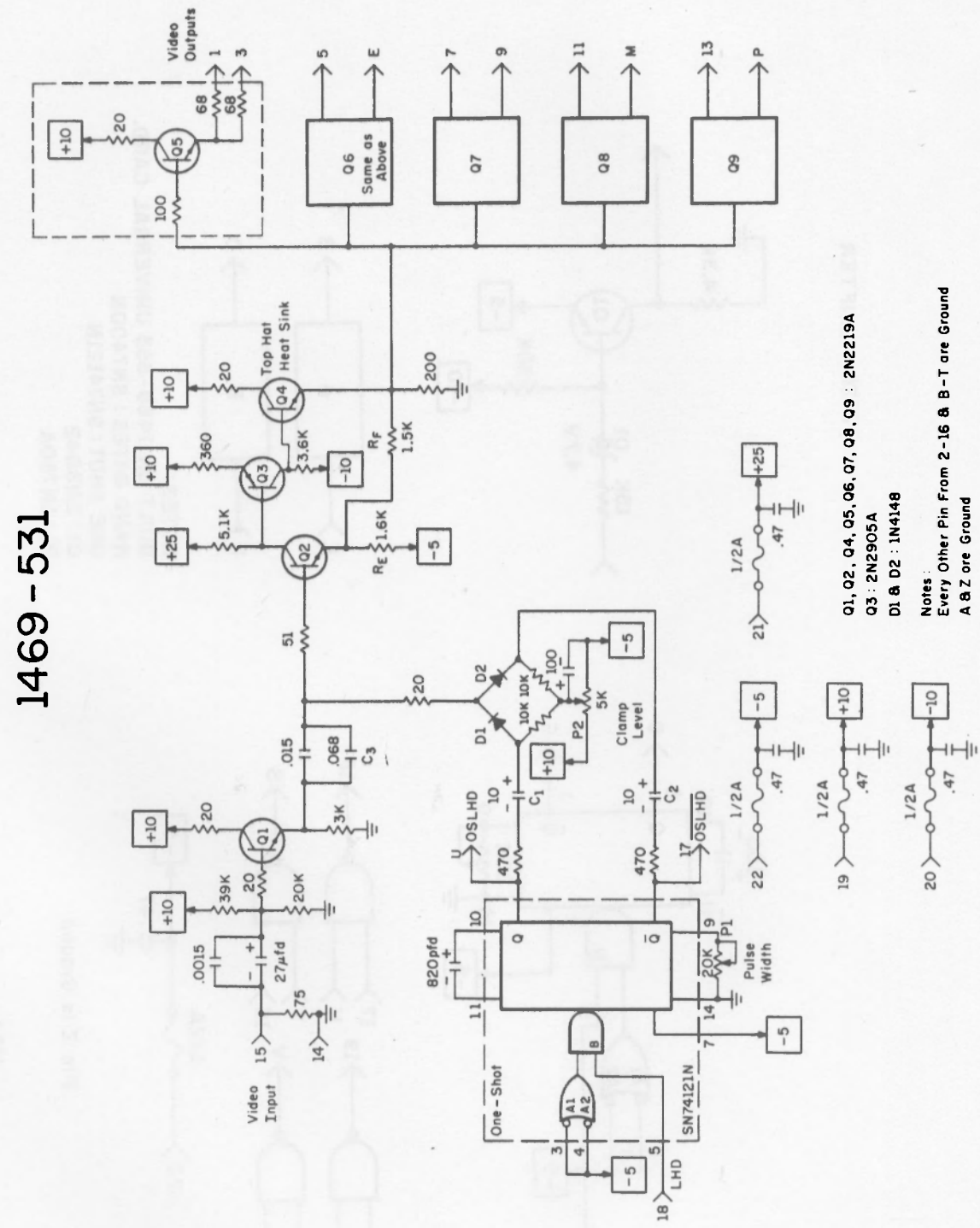


Figure 24. Video Distribution Amplifier

Capacitor C_3 is made small so that the diode clamping gate can easily charge it. A high input-impedance amplifier is used so as not to appreciably affect the charging and discharging of C_3, thereby avoiding low frequency distortion. This amplifier, composed of Q2, Q3 and Q4. is a direct-coupled voltage feedback amplifier and is discussed in references [2], [10], [11], [12], [13], [14] and [15] as well as most electronics texts. It should be mentioned here that the voltage gain A_v of such a circuit is approximately $(R_E + R_F)/R_E$; the input impedance is high ~150kΩ and the output impedance is low. Variations of this basic feedback triple are used in other parts of this project.

In the case at hand, the gain $(R_E + R_F)/R_E$ is made to be almost two so that the voltage divider between 66Ω and the 75Ω cable at the emitter of each buffer transistor (Q5 through Q9) will keep the output signal amplitudes approximately equal to the input signal amplitude. Potentiometer P2 is set such that the sync portion of the video at the outputs is clipped off when the outputs are terminated in 75Ω. P1 is adjusted so that OSLHD is slightly shorter than the camera's horizontal sync.

3. The Ultrasonic Delay Line

The Ultrasonic Delay Line was purchased from Corning Glass Company. Figure 25 shows the delay line circuit topology as it was when it arrived. One feature of this circuit is that it has automatic gain control (AGC). This feature hampered the balanced operation of the Vertical Differentiator circuit. For this reason, the delay line circuit was modified; the modified circuit, without AGC, is shown in Figure 26. The 2kΩ potentiometer should be set so that the voltage reading at TP3 is about +6 volts. This was the average voltage at TP3 before modification.

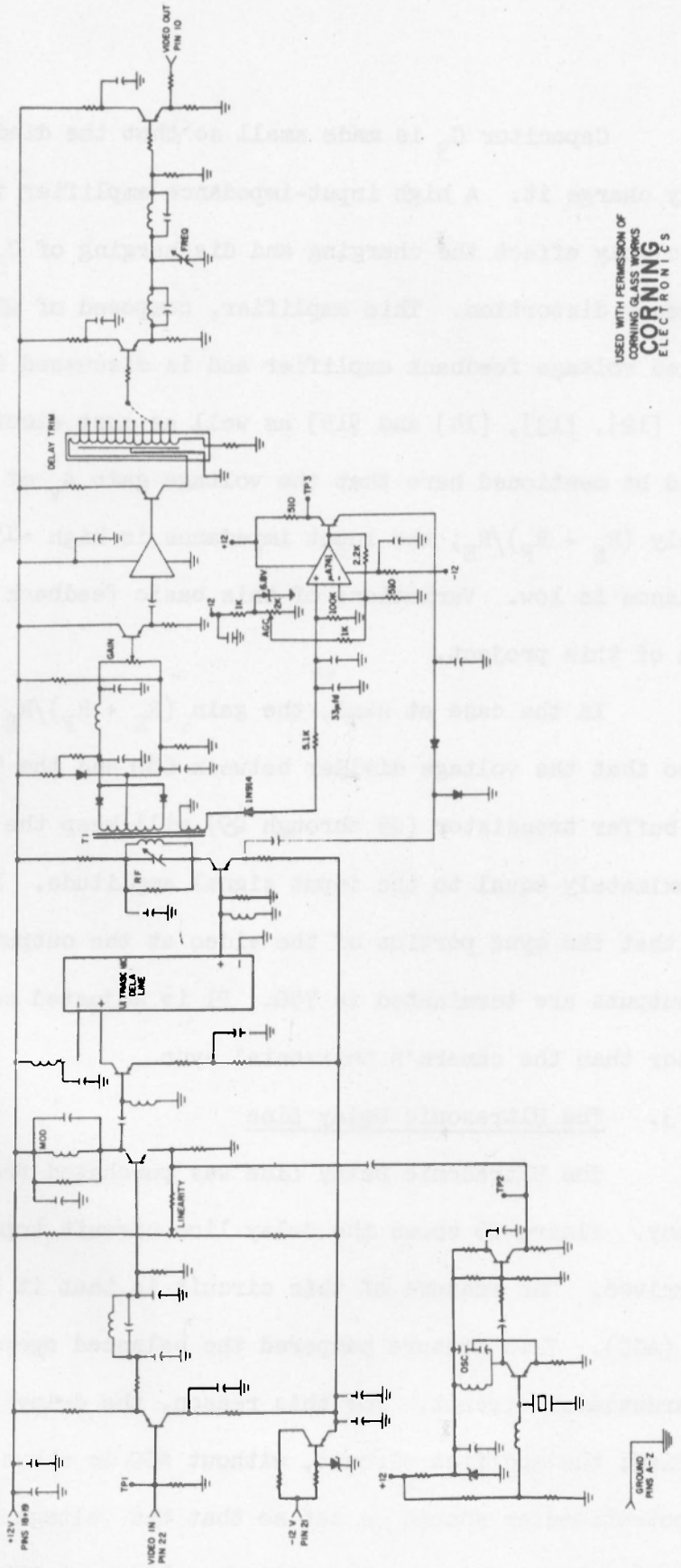


Figure 25. Ultrasonic Delay Line

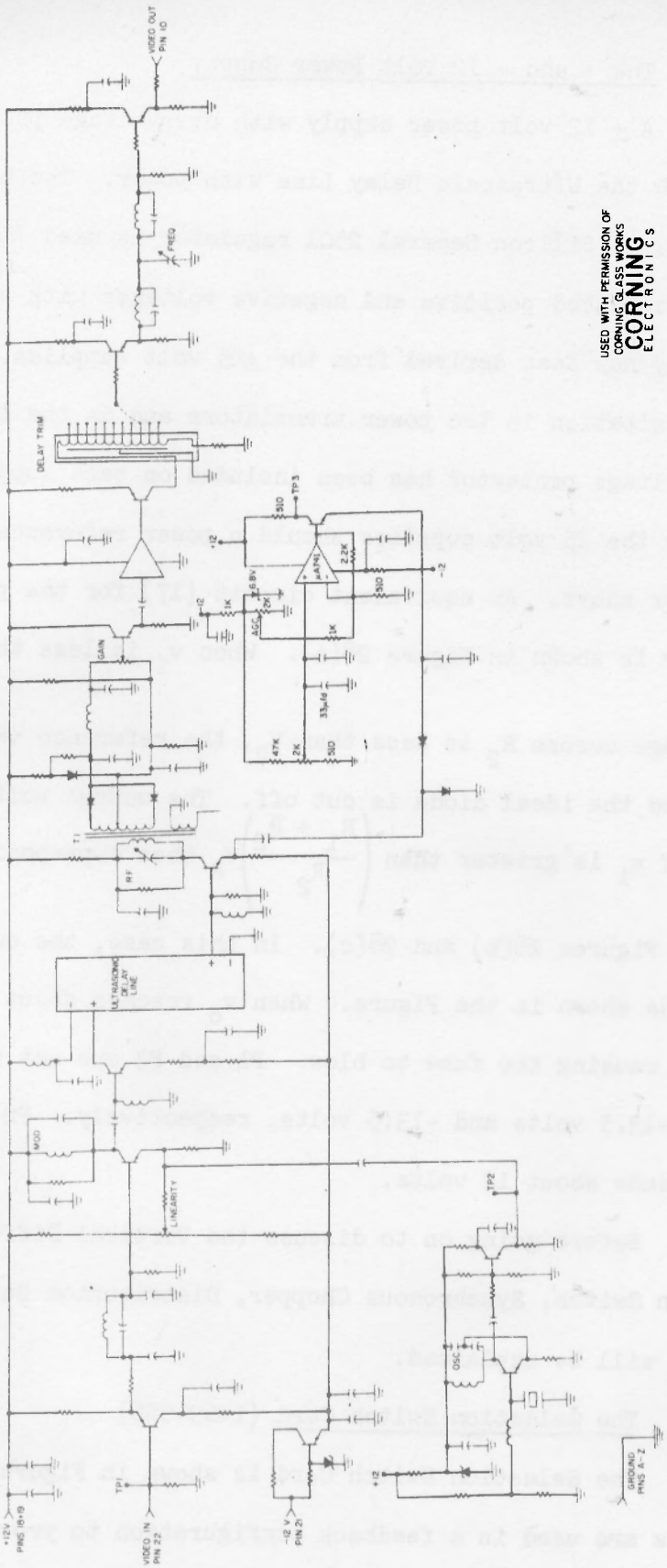


Figure 26. Modified Ultrasonic Delay Line

4. The + and - 12 Volt Power Supply

A ± 12 volt power supply with overvoltage protection was built to furnish the Ultrasonic Delay Line with power. The circuit is shown in Figure 27. A Silicon General 2501 regulator is used [16]. This regulator provides balanced positive and negative voltages with a single adjustment. The supply has been derived from the ±25 volt supplies. Diodes D1 and D2 lower dissipation in the power transistors and in the integrated circuit. An overvoltage protector has been included on each supply to protect the delay line from the 25 volt supplies should a power reference diode or power transistor short. An equivalent circuit [17] for the positive overvoltage protector is shown in Figure 28(a). When v_i is less than $\left(\frac{R_1 + R_2}{R_2}\right) V_R$, the voltage across R_2 is less than V_R, the reference voltage of the reference diode, and the ideal diode is cut off. The output voltage v_o is zero in this case. If v_i is greater than $\left(\frac{R_1 + R_2}{R_2}\right) V_R$ then superposition may be used as shown in Figures 28(b) and 28(c). In this case, the output voltage v_o equals $e_1 + e_2$ as shown in the Figure. When v_o reaches about .5 volt, the SCR will trigger, causing the fuse to blow. P1 and P3 are set to trigger SCR1 and SCR2 at +13.5 volts and -13.5 volts, respectively. P2 is set so that each output reads about 12 volts.

Before going on to discuss the Vertical Differentiator and Logic, the Selection Switch, Synchronous Chopper, Distribution Buffer and Logical Blanking circuits will be explained.

5. The Selection Switch Card (1469-528)

The Selection Switch Card is shown in Figure 29. Open collector inverters are used in a feedback configuration to provide a contact bounceless switch signal. This circuit [18] is used in the D.C.S. Logic Laboratory modules.

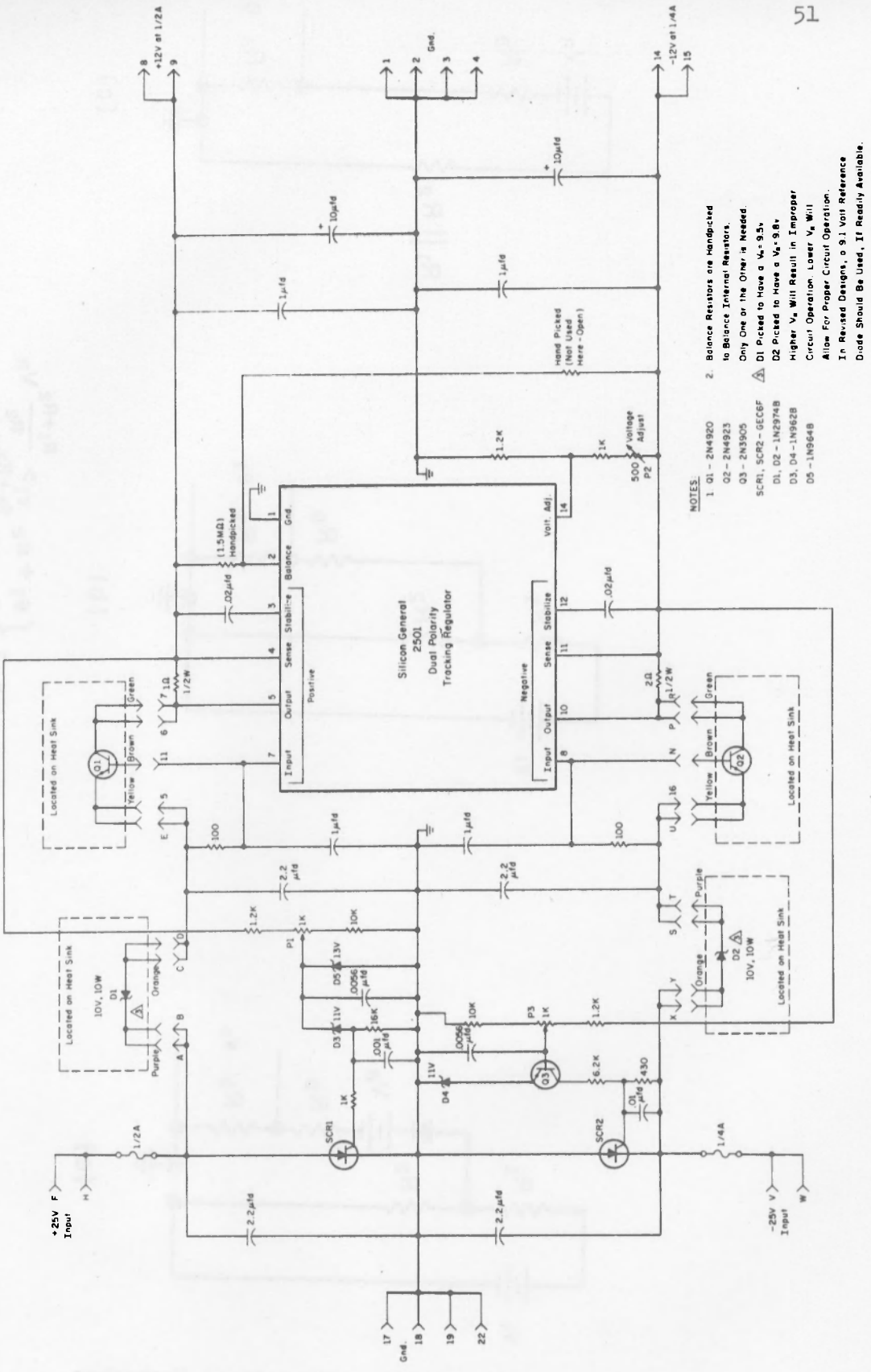


Figure 27. + and - 12 Volt Power Supply

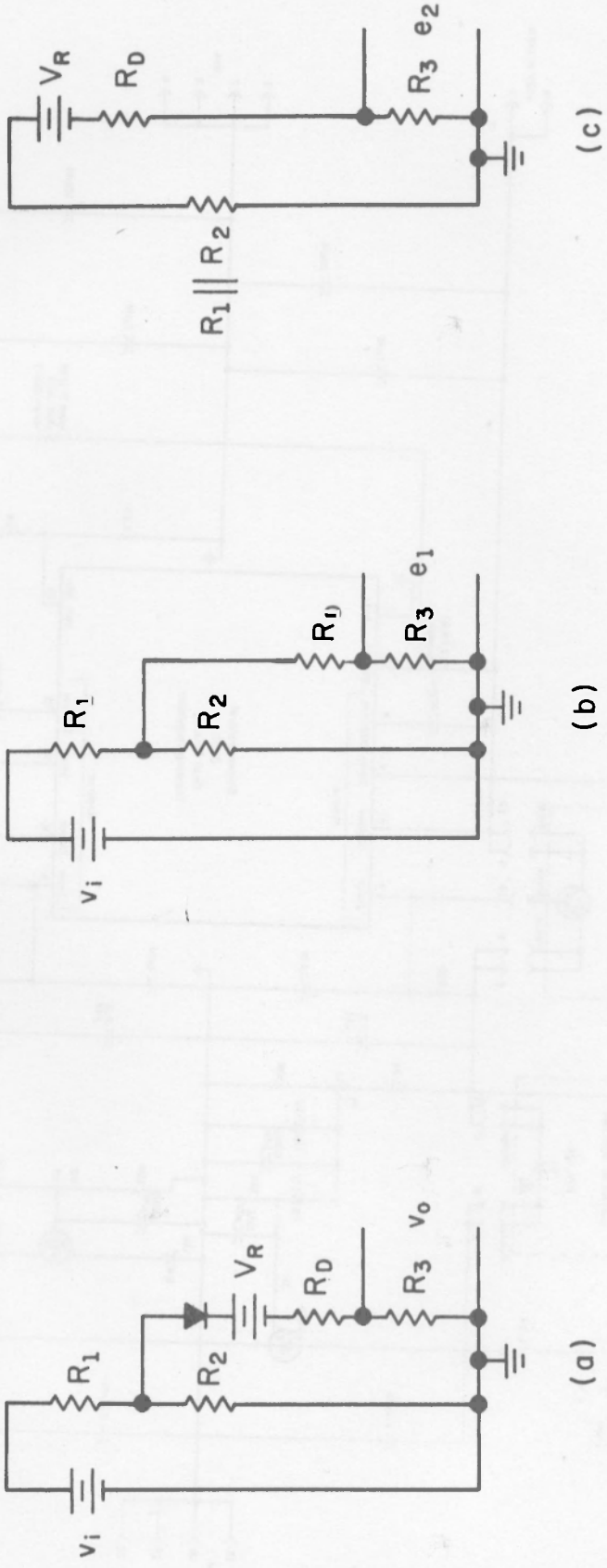


Figure 28. Positive Overvoltage Protector

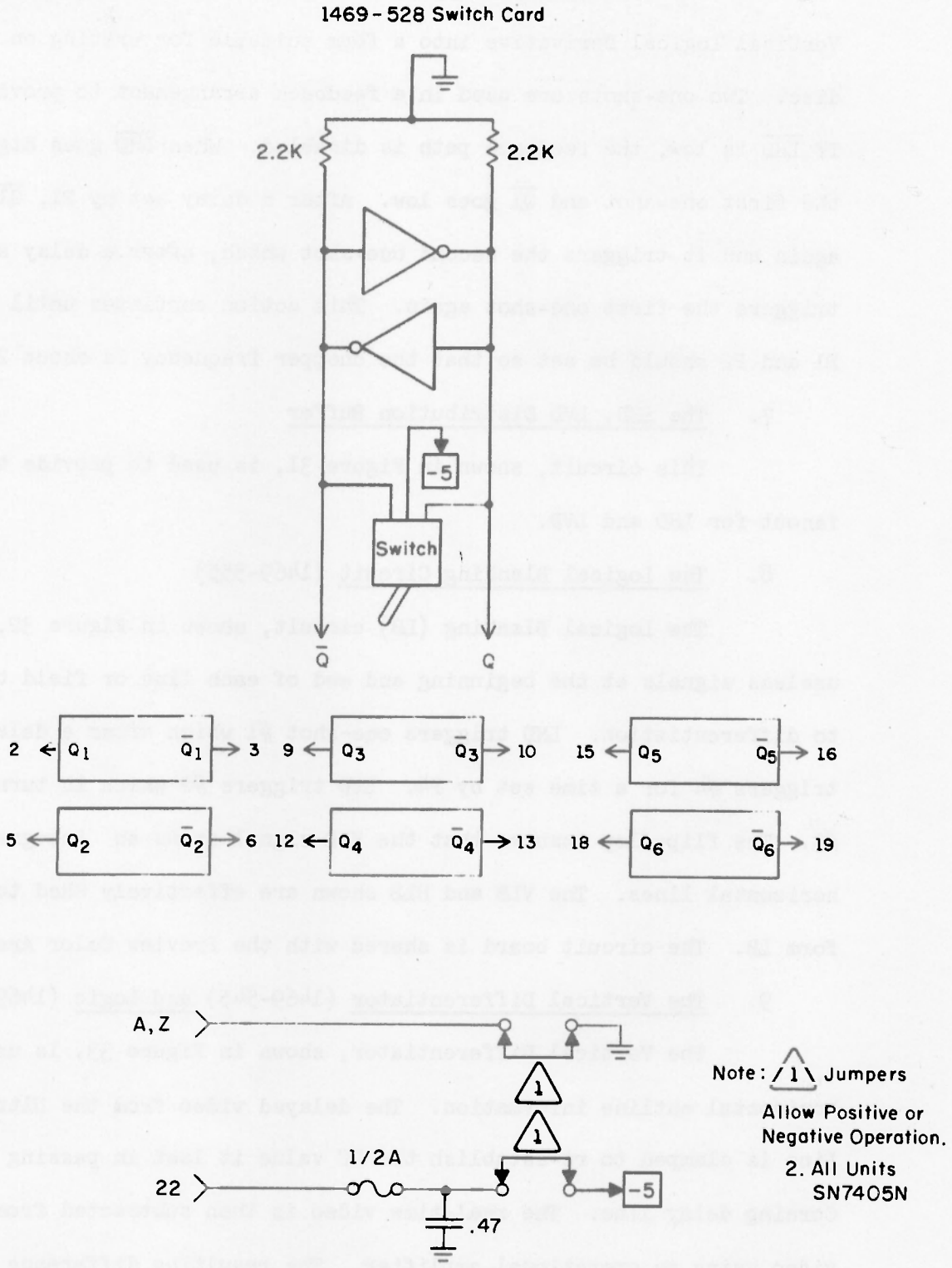


Figure 29. Switch Card

6. The Synchronous Chopper

The Synchronous Chopper, shown in Figure 30, is used to chop the Vertical Logical Derivative into a form suitable for writing on the video disc. Two one-shots are used in a feedback arrangement to provide oscillation. If $\overline{\text{LHD}}$ is low, the feedback path is disabled. When $\overline{\text{LHD}}$ goes high, it triggers the first one-shot and $\overline{\text{Q1}}$ goes low. After a delay set by P1, $\overline{\text{Q1}}$ goes high again and it triggers the second one-shot which, after a delay set by P2, triggers the first one-shot again. This action continues until $\overline{\text{LHD}}$ goes low. P1 and P2 should be set so that the chopper frequency is about 2.8 MHz.

7. The LHD, LVD Distribution Buffer

This circuit, shown in Figure 31, is used to provide the necessary fanout for LHD and LVD.

8. The Logical Blanking Circuit (1469-555)

The Logical Blanking (LB) circuit, shown in Figure 32, blanks out useless signals at the beginning and end of each line or field that arise due to differentiation. LHD triggers one-shot #1 which after a delay set by P1 triggers #4 for a time set by P4. LVD triggers #2 which in turn triggers #3. The flip-flop insures that the VLB signal spans an integral number of horizontal lines. The VLB and HLB shown are effectively ORed together to form LB. The circuit board is shared with the Preview Color Area circuit.

9. The Vertical Differentiator (1469-545) and Logic (1469-546)

The Vertical Differentiator, shown in Figure 33, is used to provide horizontal outline information. The delayed video from the Ultrasonic Delay Line is clamped to re-establish the DC value it lost in passing through the Corning delay line. The real-time video is then subtracted from the delayed video using an operational amplifier. The resulting difference signal is

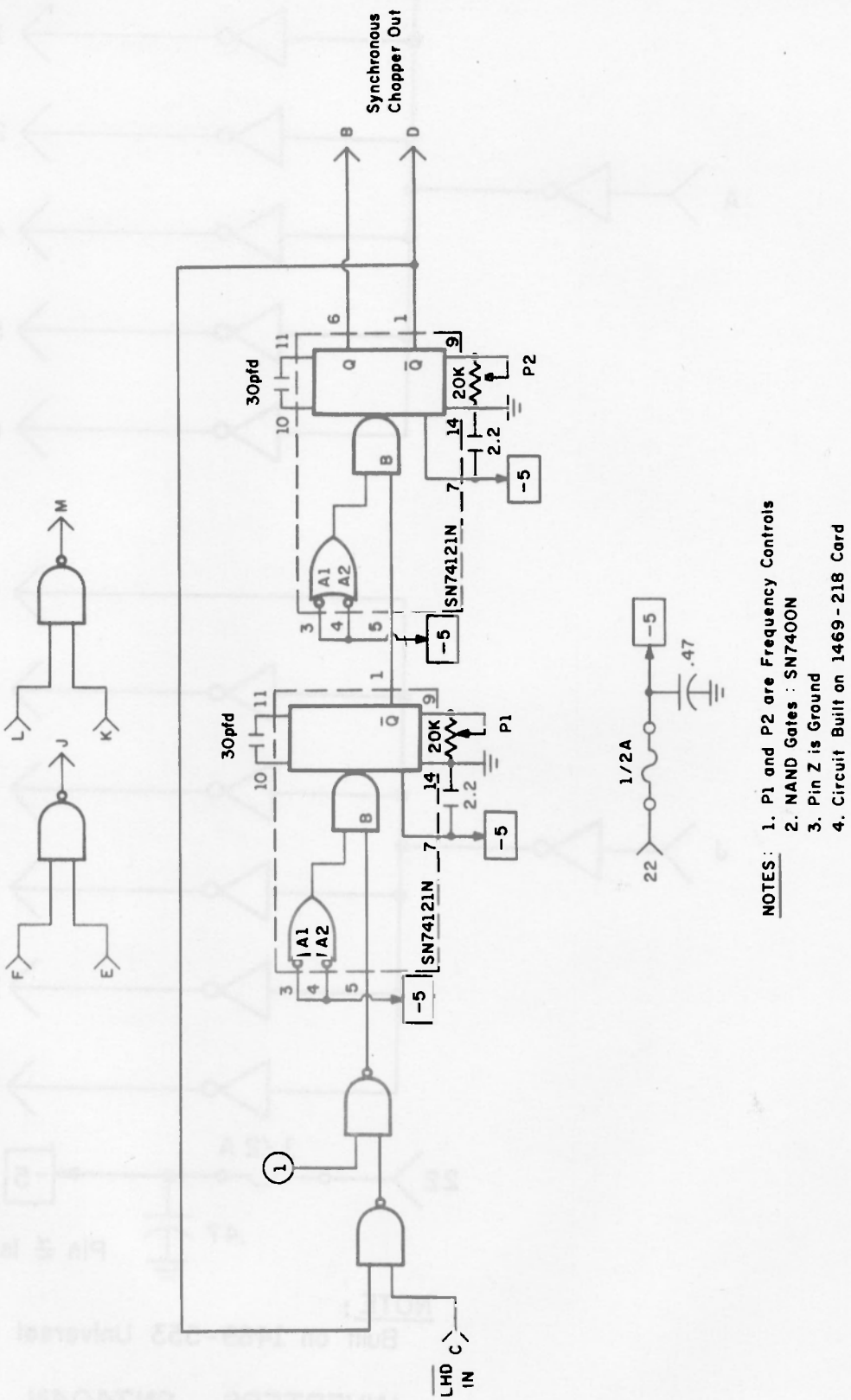


Figure 30. Synchronous Chopper

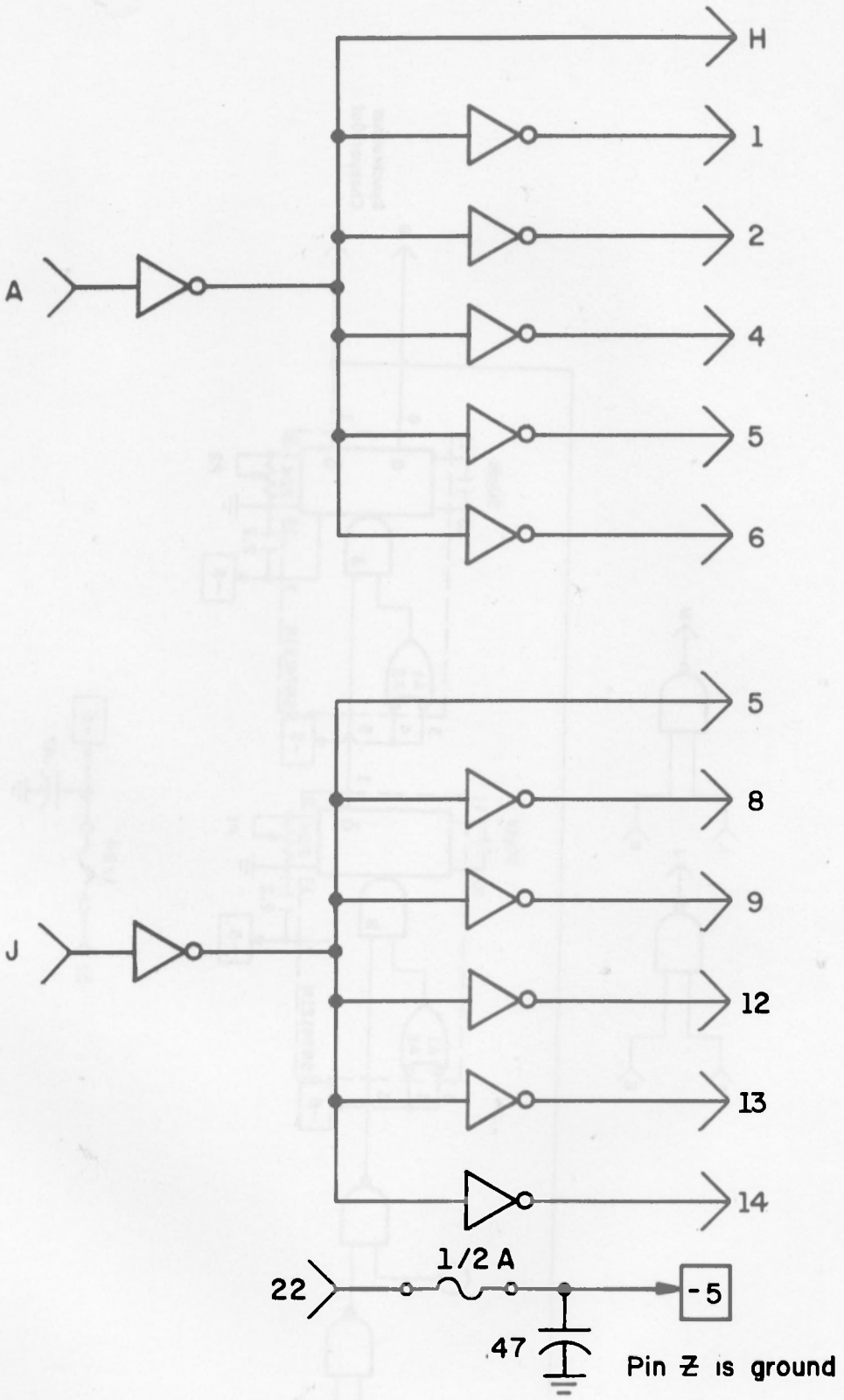


Figure 31. LHD, LVD Distribution Buffer

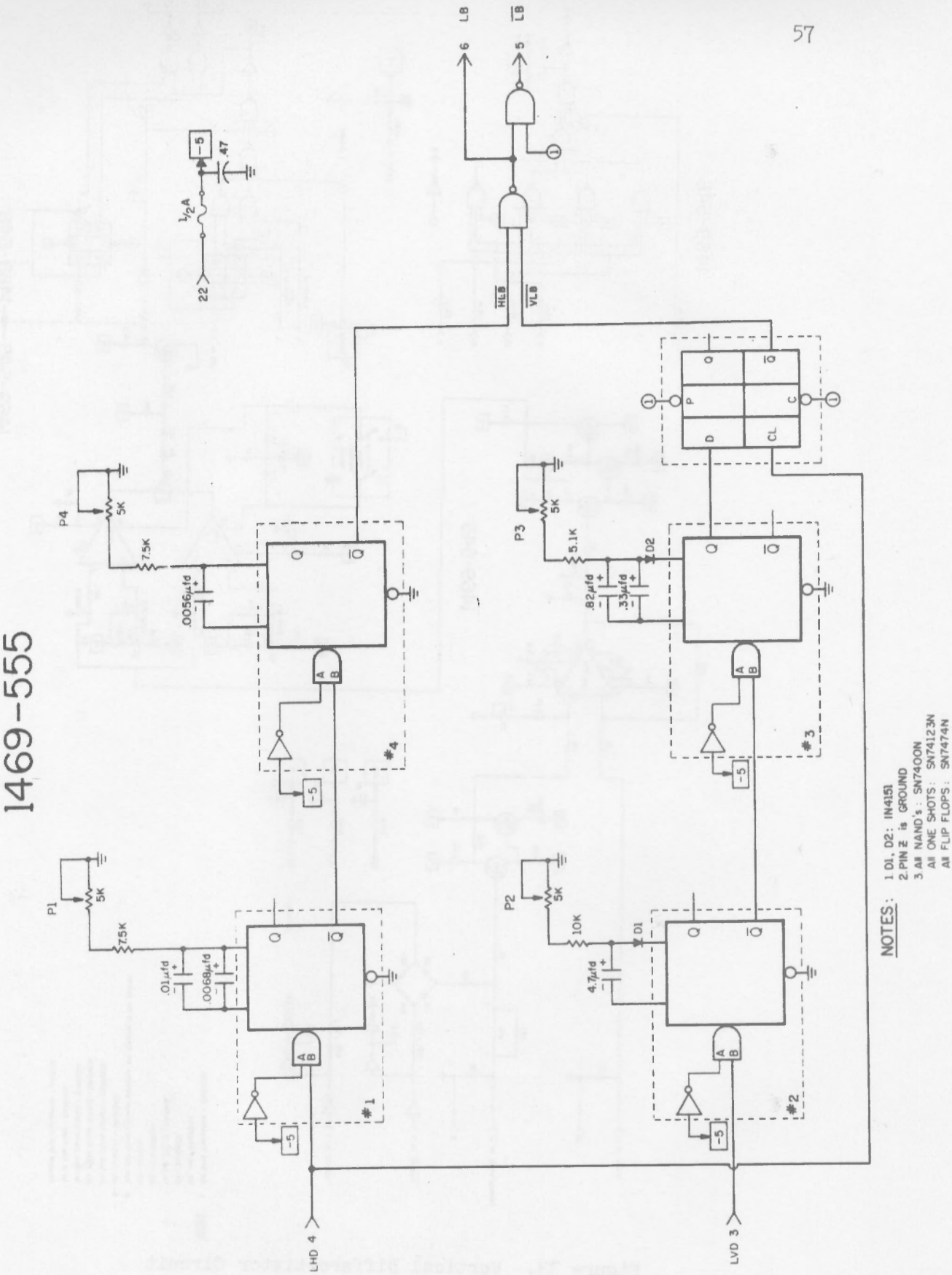


Figure 32. Logical Blanking Circuit

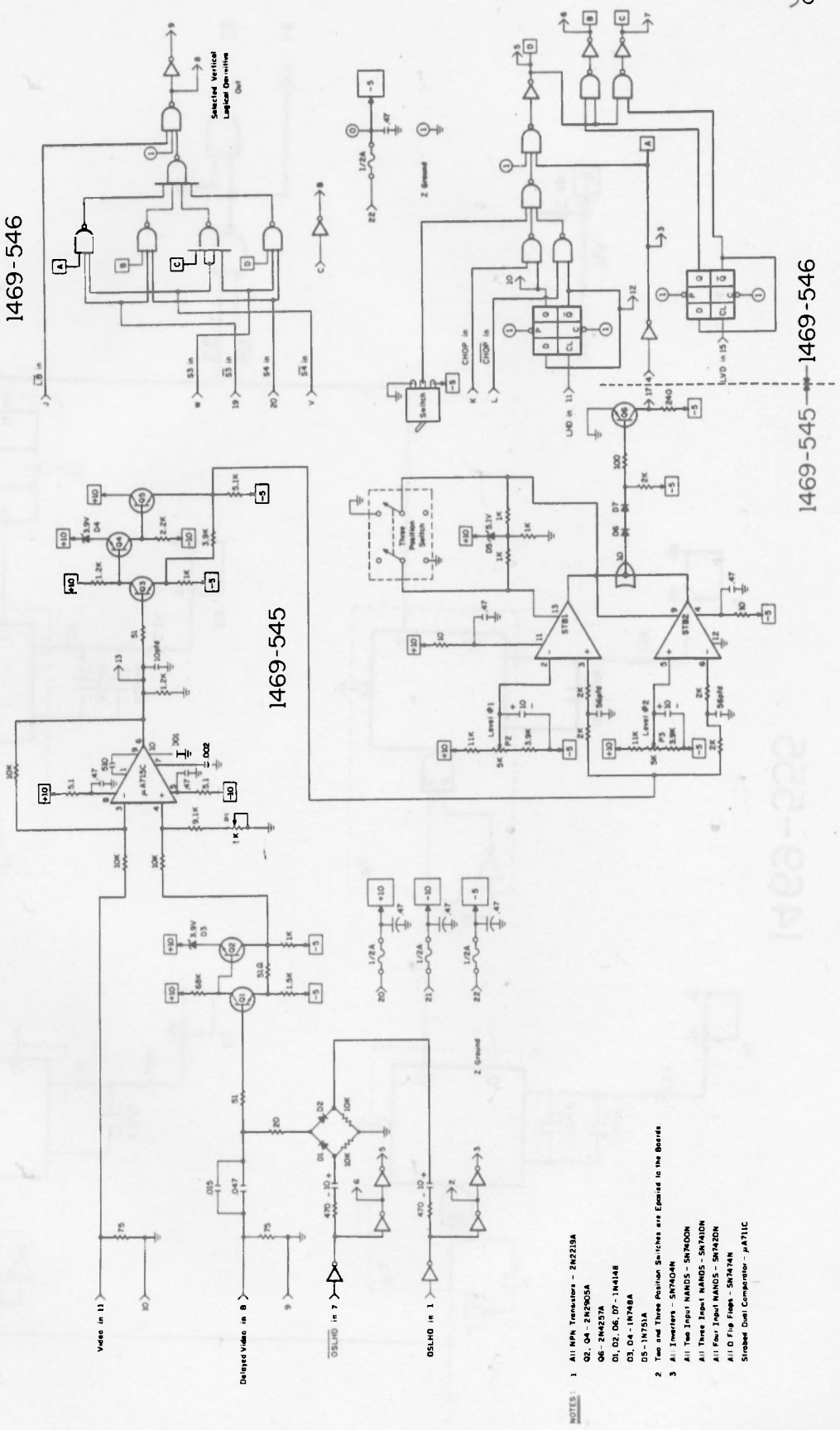


Figure 33. Vertical Differentiator Circuit

then amplified with a feedback triple before passing on to a Fairchild μA711C strobed dual comparator. A T filter is used to bypass high frequency components of the difference signal. The signal enters the plus terminal of one comparator and the minus terminal of the other. The voltage dividers at the other inputs set the comparison levels. The position of the three position switch sets the strobe voltages. From Table 2, we see that the switch selects either a positive or negative single-sided threshold (up and down) or a double-sided threshold (center position). The wire ORed output is then level-shifted to standard TTL levels.

The top photo in Figure 34, shows about 16 lines of video and the corresponding difference signal. The scene viewed was a square white card on a black background. The bottom photo shows the real-time video, the delayed video, and the difference signal over a period of almost a field.

The Vertical Differentiator Logic, also shown in Figure 33, is on a 1469-546 card. The inverted level-shifted dual comparator signal is chopped if the center terminal of the two-position switch is grounded. The chopping signals come from the Synchronous Chopper (see Figure 30). The chopping is done using CHOP for one line and $\overline{\text{CHOP}}$ for the next (timewise) so that an outline stored on the disc won't have any holes in it. The signal at common point A is the unchopped original signal while that at D is either chopped or not depending upon the two-position switch position. The signals at common points B and C are the same as at D except that either the odd or the even field is blanked out. Switch inputs from the Switch Card (see Figure 29) and the common points A, B, C and D go to a decoding circuit which selects one of the four common points A through D as the output. This signal is then blanked

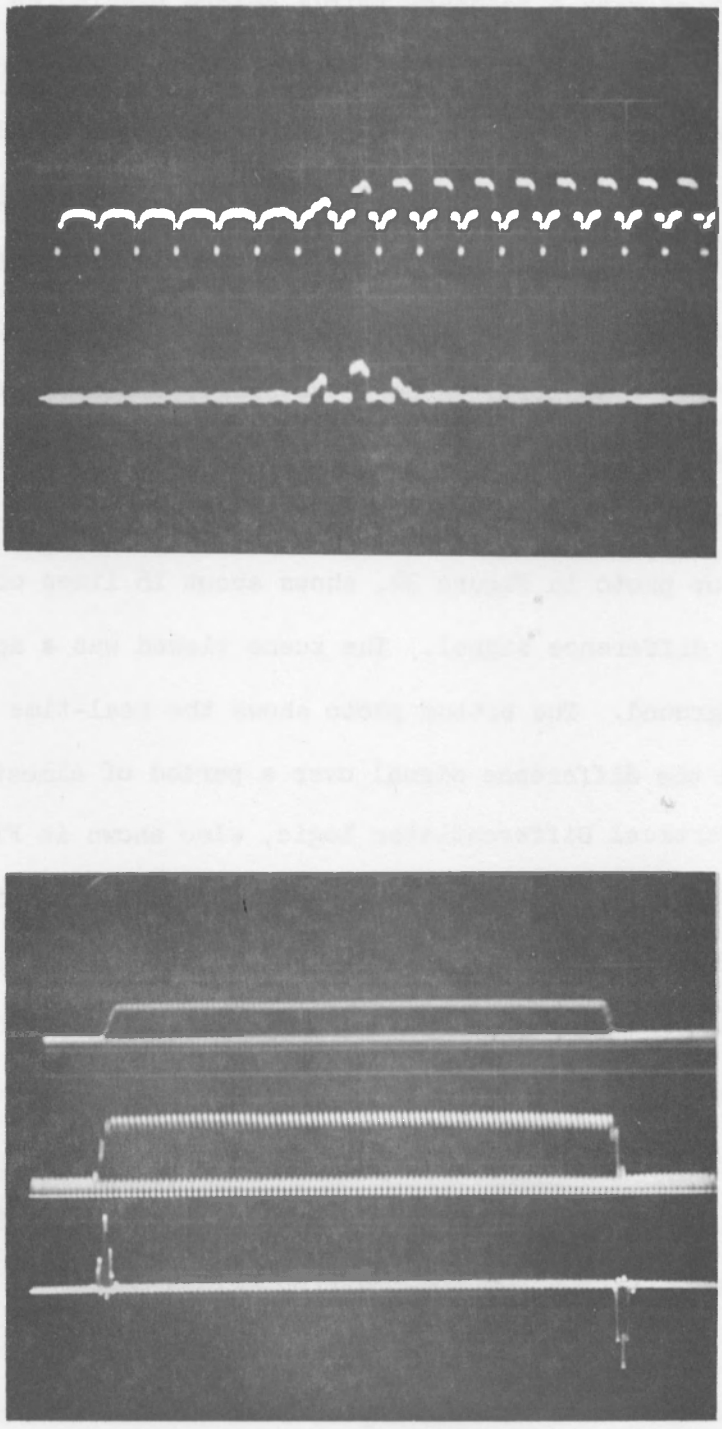


Figure 34. Sample Difference Signal

during horizontal and vertical blanking with the output of the Logical Blanking (LB) circuit (see Figure 32) before passing through the final output.

10. The Horizontal RC Filter Differentiator (1469-474)

Next, the two horizontal differentiators will be discussed. The RC Filter Differentiator, shown in Figure 35, was built experimentally. The design criteria were

(1) to duplicate a line drawing drawn on a blackboard

and (2) to form the outline of scenes composed of contrasty solid colors.

In the drawing, the chain composed of Q1, Q2 and Q3 forms a high frequency-response differentiator. The top trace in Figure 36 shows the video input and the bottom shows the output at the collector of Q3. Q1 and Q4 form a derivative of lower frequency picture components and need not be used except for solid objects. The comparator after Q3 is set to detect positive signal deviations while that after Q4 detects negative deviations. Q5 and Q6 level shift the comparator output to standard TTL logic levels for use by the one-shots.

11. The Horizontal Delay Line Differentiator (1469-536) and Logic (1469-537)

For the sake of symmetry, it was of interest to build a delay line differentiator for the horizontal derivative as well. An analysis of the use of a shorted delay line as a differentiator is given in Appendix A.

The Horizontal Delay Line Differentiator with Logic is shown in Figure 37. The video signal is amplified by about six using the feedback amplifier made up of stages Q1 through Q6. The characteristics of a similar

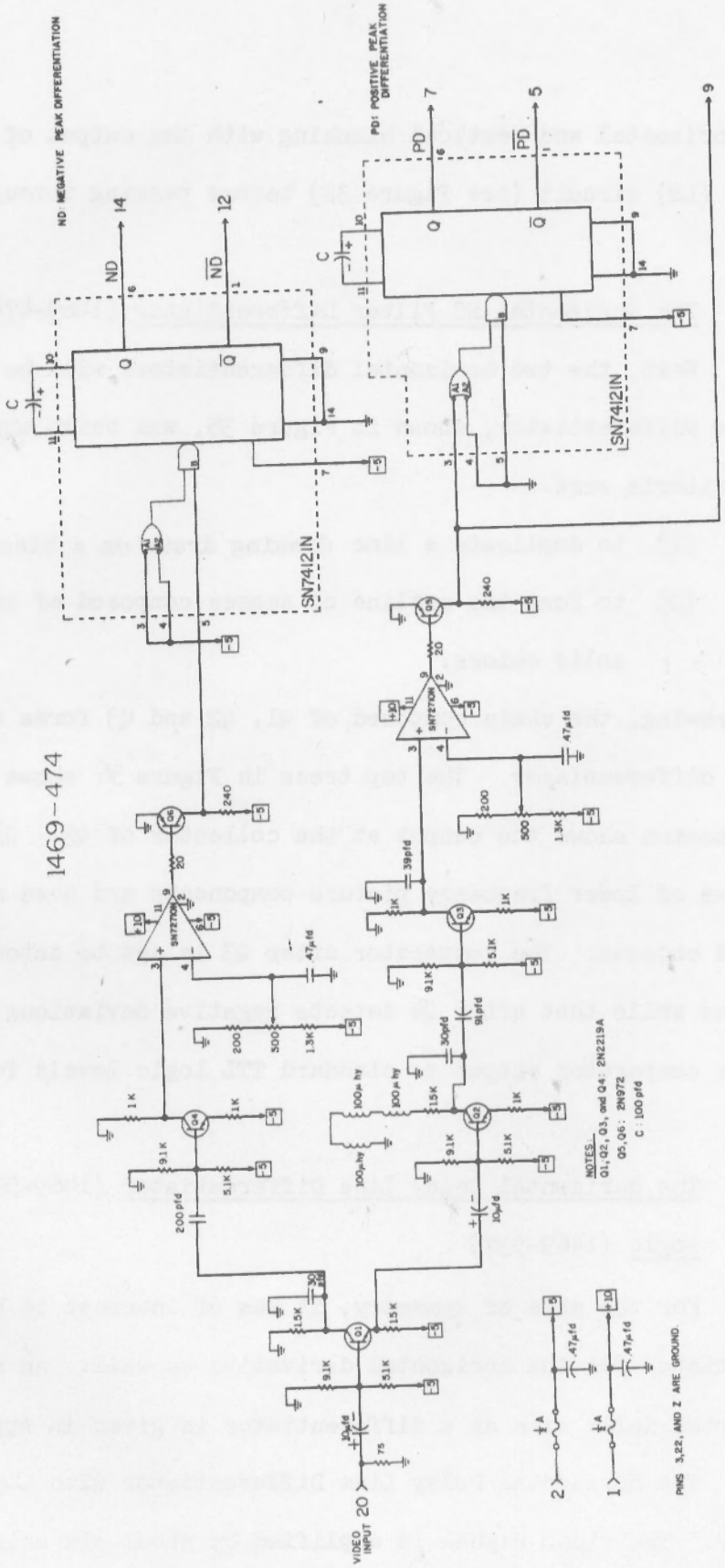


Figure 35. Horizontal RC Filter Differentiator

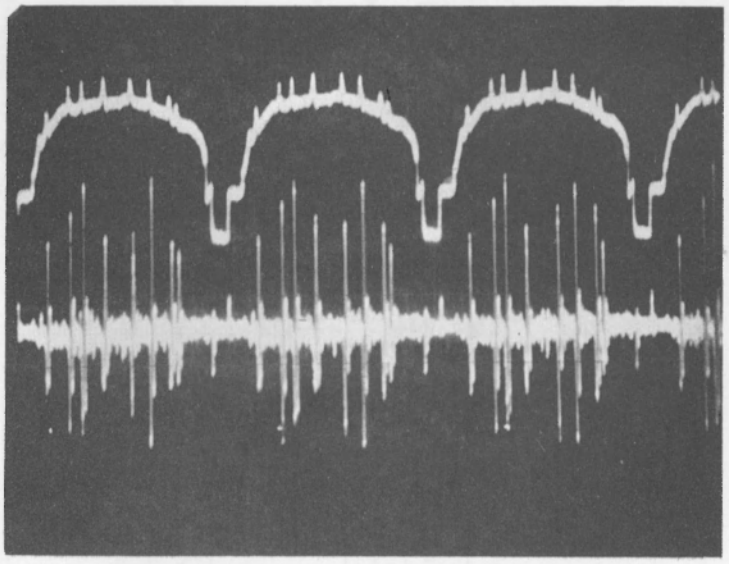


Figure 36. Sample RC Filter Differentiator Input/Output Voltages

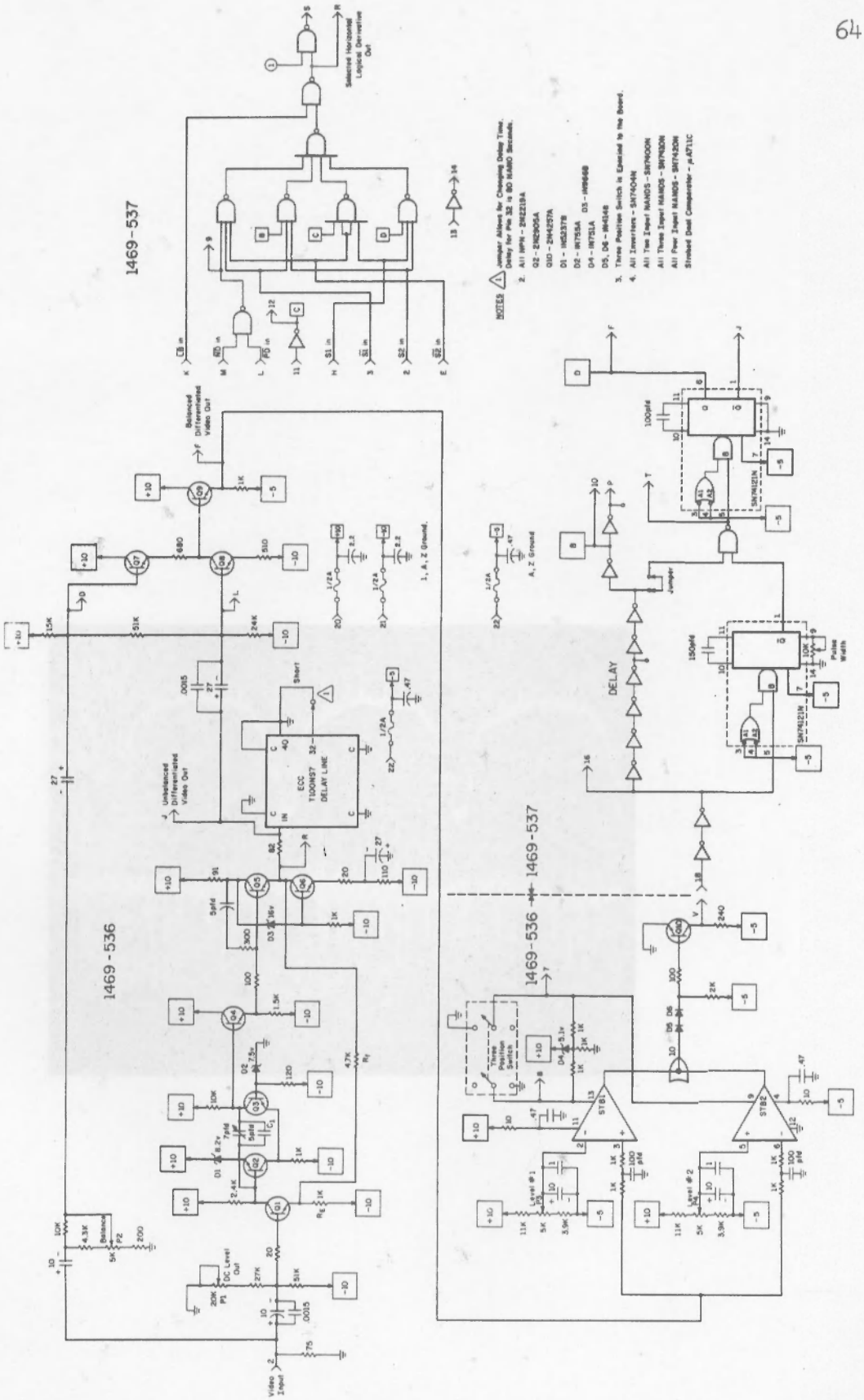


Figure 37. Horizontal Delay Line Differentiator and Logic

amplifier are calculated in Reference [30]. Potentiometer P1 adjusts the output DC level. The input stage Q1 is an emitter follower with its emitter tied to the feedback path. Q2 and Q3 form a complementary cascode circuit with an effective adjustable Miller feedback capacitance C_1. The bandwidth of the amplifier may be varied by adjusting C_1. Emitter follower Q4 serves to lower the impedance seen by the output stage Q5-Q6. An analysis of a similar output stage is given in Reference [31]. Basically, Q5 serves as a source of current for voltages above ground and Q6 a sink for those below. If the emitter of Q4 is at least a diode drop above ground, then Q5 is pushing current into the load. As the input voltage goes up, the voltage drop across the 91Ω collector resistor reduces the bias on Q6 through D3. As the input voltage falls below ground, Q5 is turned off and Q6 is turned on through D3. Q6 then serves as a current sink. This amplifier provides a high quality 10 volt peak-to-peak video signal to the delay line. The one-way delay time of the delay line was chosen by experiment to be 80 nsec. Appendix A shows that the constraint for a delay line differentiation to be close to the derivative is $\omega T < .17$ radians. This gives

$$f_H = \frac{\omega_H}{2\pi} \sim \frac{.17}{2\pi \times 80 \times 10^{-9}\text{s}} \sim 340 \text{ kHz}.$$

For frequency components higher than f_H, the difference between the real-time and the delayed video components essentially subtracts out the low frequency hump, but retains the higher frequency pulses and their echoes. The result of a single-sided threshold appears much like the original line drawing. For double-sided thresholds, echoes from high frequency pulses are separated on the screen from the original by a distance corresponding to 2T. The lower frequency pulses are effectively differentiated, and the resultant output takes

on the appearance of an outline. Q7 and Q8 form a difference circuit used for balancing the delay line output to account for the attenuation. This is discussed in Appendix A. P2 determines the amount of input signal that is subtracted from the unbalanced differentiated video. Capacitive coupling is used here to simplify circuit design. Emitter follower Q9 drives the comparator inputs. A sample of delay line differentiation is shown in Figure 38. The top line is the input video and the bottom line is the voltage at the emitter of Q9. A T filter is used on each comparator input to bypass high frequencies. P3 and P4 set the threshold levels and the 3-position switch controls the strobe inputs for a single- or double-sided threshold (see Table 2). The comparator output is level shifted to TTL logic levels by D5, D6 and Q10. The logic card (1469-537) performs the double line correction and the signal selection. The correction scheme was discussed in Chapter II (see Figure 6 and Section II.B.1.f). The selector circuit is identical to that discussed in connection with the Vertical Differentiator. The output for a given switch position is given in Table 1 and is labelled the Horizontal Logical Derivative (HLD).

12. The Video Gate (1469-554) with L/V Converter

The Video Gate circuit is shown in Figure 39 along with a L/V Converter that was etched on the same card for economy. A similar circuit is discussed in Reference [30]. The inverters used here are open collector inverters with 30 volt minimum breakdown voltages. The video input is pin 3 and the gate input is pin 11. If the gate signal goes high (ground), then Q2 will be turned on and the video signal will pass on to the outputs. If the gate signal goes low (-5), then Q2 will be turned off, D1 and D2 will be turned off and D3 will be on, thus not allowing the video to pass to the outputs.

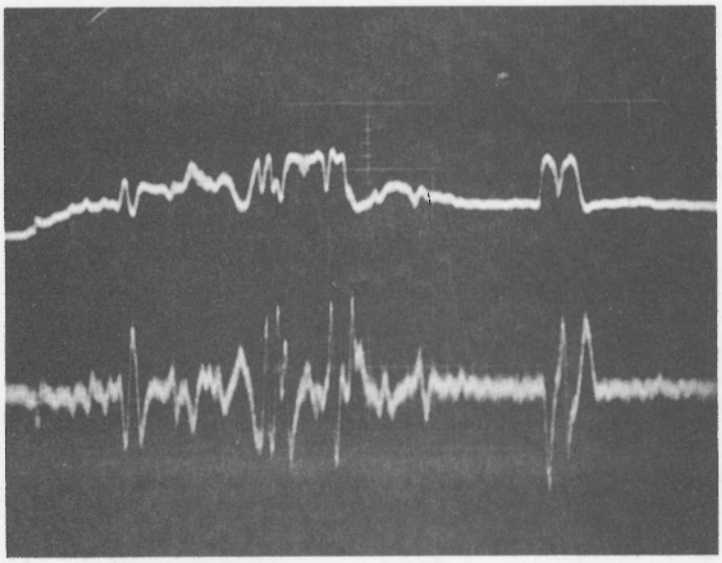
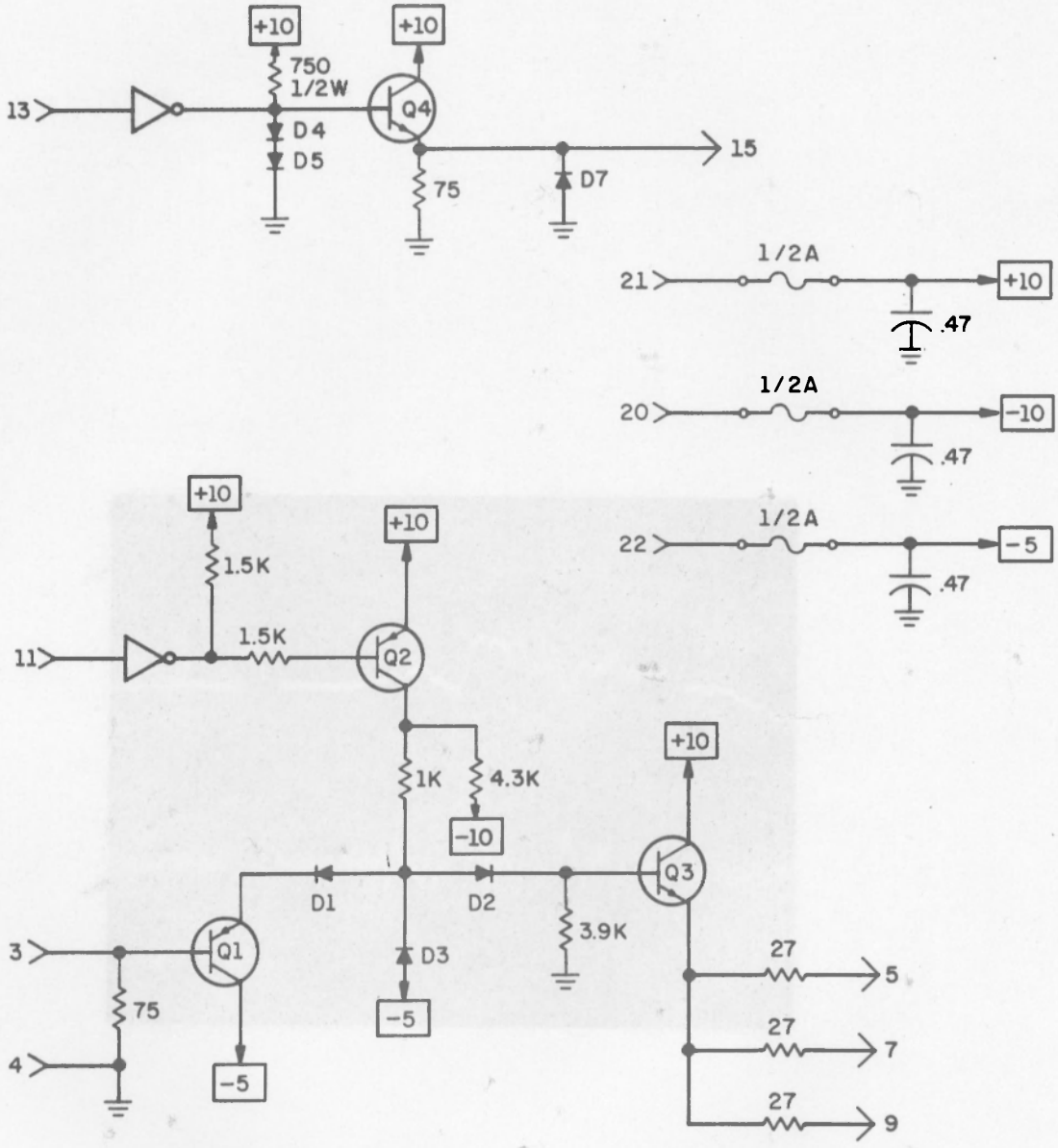


Figure 38. Sample Horizontal Delay Line Differentiator Input/Output Voltages



NOTES

1. Q1: 2N2905A
   Q2: 2N3905
   Q3,Q4: 2N2219A
   D1 - 1N995
   D2,D3 - 1N4151
   D4,D5 - 1N4148
2. PINS 1,2,4,6,8,10,16 are ground.
3. INVERTER: SN7406N

Figure 39. Video Gate with L/V Converter

13. The One Frame Gate

The One Frame Gate, shown in Figure 40, provides a gating signal for gating the outline information onto the disc. When the "STORE OUTLINE" switch on the front panel is depressed, the Gate Outline (GO) output goes high for the duration of two fields. The resistor-capacitor circuits at the switch panel and on the card provide a one-shotted pulse to the preset terminal of the flip-flop when the "STORE OUTLINE" button is pushed. The 220Ω resistor was chosen to keep the steady state voltage at pin 14 equal to about -4.65 volts (logical zero). The 4.7 μfd capacitor was chosen to provide an output pulse width of about 2.5 msec. The .47 μfd capacitor is used to suppress coupled transients that would otherwise trigger the gate. The details of the Moore circuit design are given in Appendix B. This completes descriptions of the outlining circuitry.

D. The Shading Circuitry

The shading circuitry described below has been added or modified for the ATC - Mark II. The reader should refer back to the System Block Diagram, Figure 11, and to the Video and Control Logic Block Diagram, Figure 20, to re-orientate himself. The control signals for the shading circuitry originate from the shading potentiometers located at the Control Panel shown in Figure 14. The potentiometer terminals are wired into the Display Console Junction Box, shown in Figure 15, where they go to the Range and Width Card, shown in Figure 17. The outputs of the Range and Width Card are voltages corresponding to the potentiometer settings. These voltages labelled RS, GS, and BS (for red, green and blue shading), are wired into the Video and Control Logic Block Diagram, as shown in Figure 20, where they are shown going to the Modulators*.

*The Modulators are really just clippers, but are referred to throughout as Modulators.

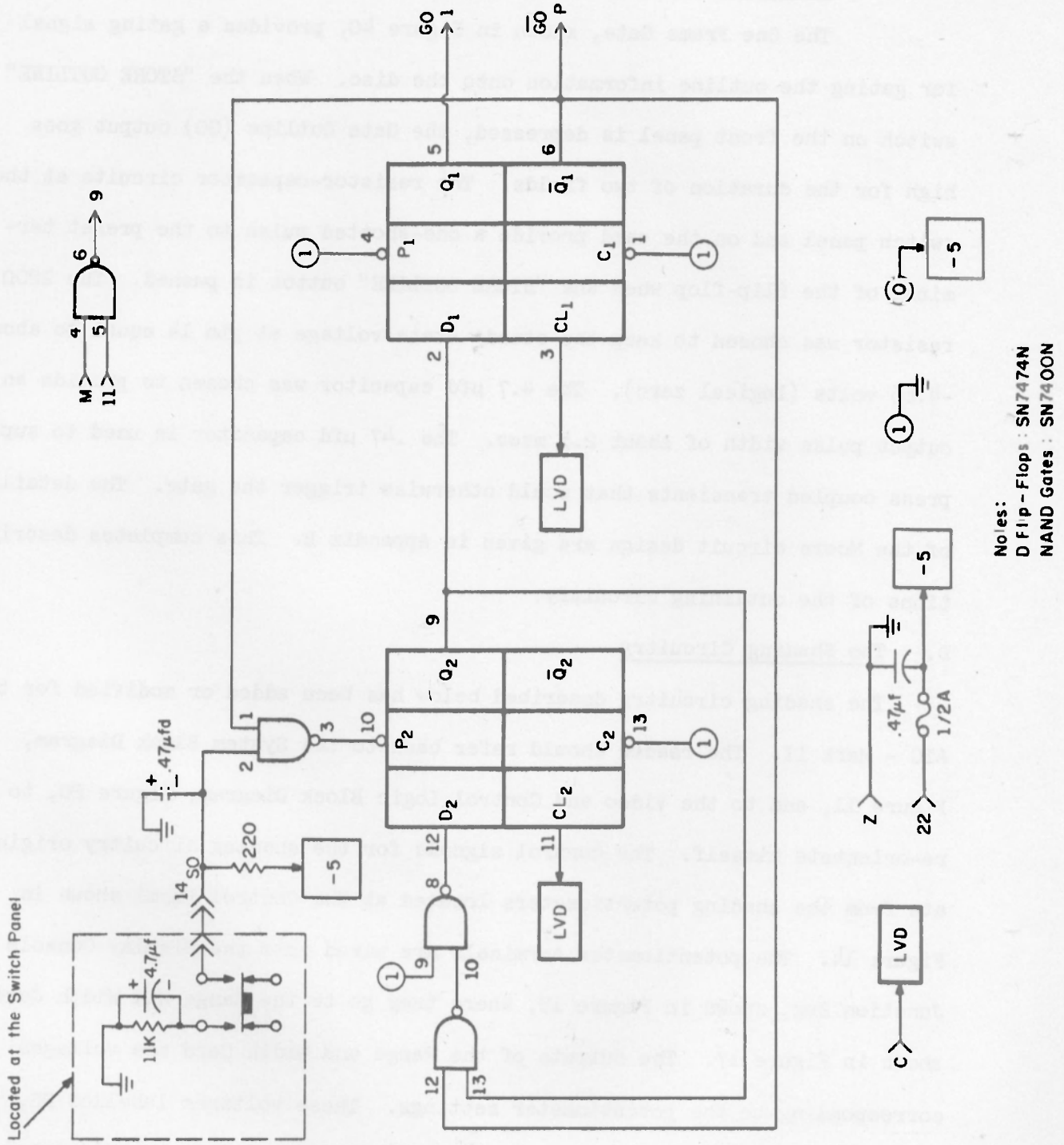


Figure 40. One Frame Gate

Each Modulator block is controlled by its respective shading voltage and has two modulators in it. One modulation signal writes on the disc and the other provides a preview color signal when the "PREVIEW COLOR" button is depressed. The area of screen used for previewing the color is adjustable by varying potentiometers on a Preview Color Area circuit card. The preview color modulator signal goes to the Video Adders, as shown in Figure 20. The preview color circuitry is necessary for the operator to correlate a potentiometer position with a visual intensity. The signals from the Modulators that go to the disc are chopped at about 3MHz by the disc's chopper before being written on the disc's surface. The signals from the disc's read heads are amplified using Disc Read Amplifiers operating in the Class A mode. The amplified color signals then go to the Demodulators and Video Adders, as shown in Figure 20, before going to the monitor.

1. The Preview Color Area Circuit (1469-555)

The Preview Color Area circuit, shown in Figure 41, is built on a card with the Logical Blanking circuit. The two circuits are very similar, except for specific timing values. See the description of the Logical Blanking circuit and Figure 32 for an explanation. Although this circuit is part of the shading circuitry, it is included in the Outlining Circuitry Block Diagram, Figure 22.

2. The Modulator (1469-556)

Three identical Modulators (A, B, C) and a Logic to Video Converter (D) are all etched on one card (1469-556), as shown in Figure 42. The shading voltage for each Modulator appears at the emitter of Q1. When the write gate signal is low (~ -5 volts), Q2 acts basically as an emitter follower and the voltage at the emitter of Q3 is nearly the shading voltage. When the write

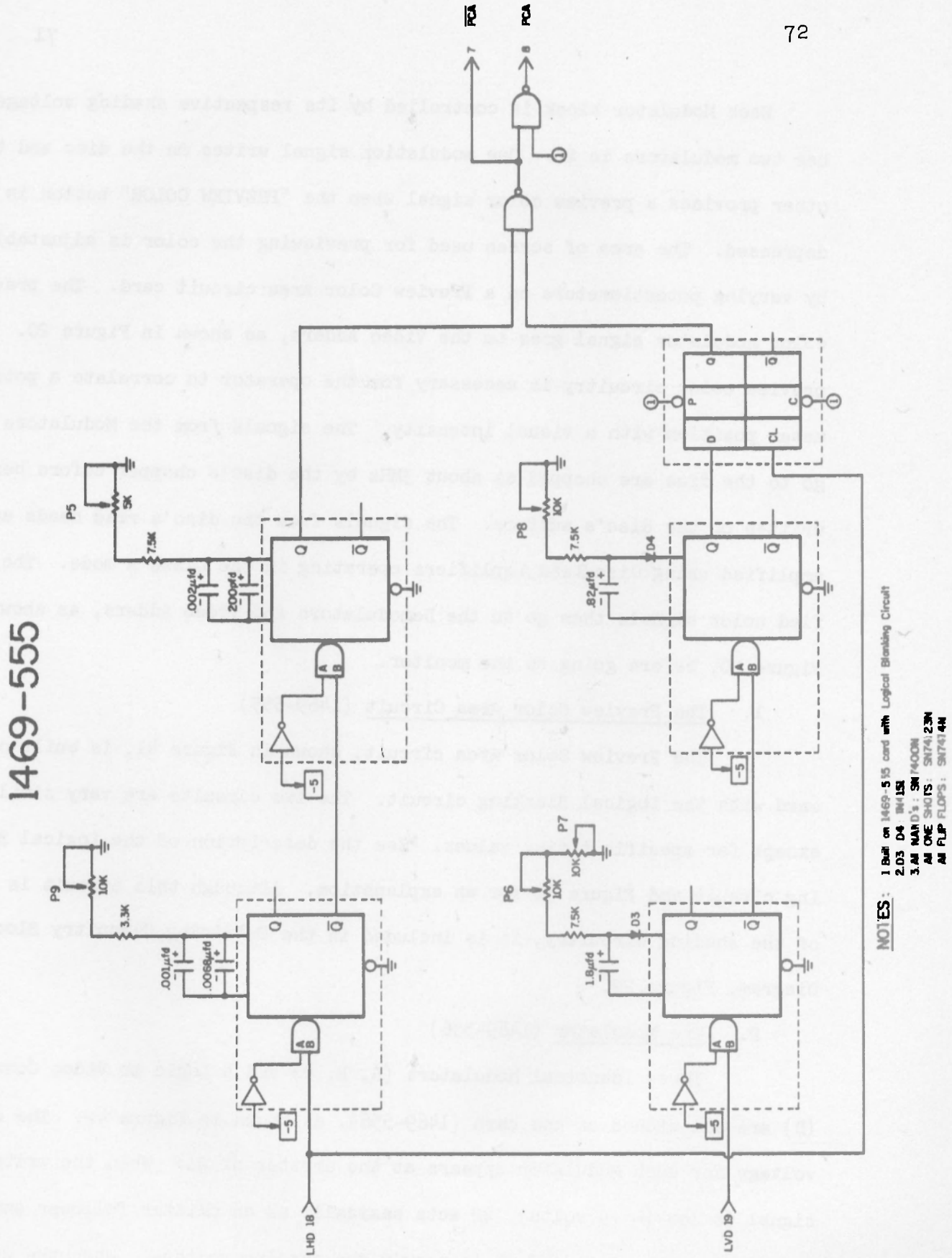


Figure 41. Preview Color Area Circuit

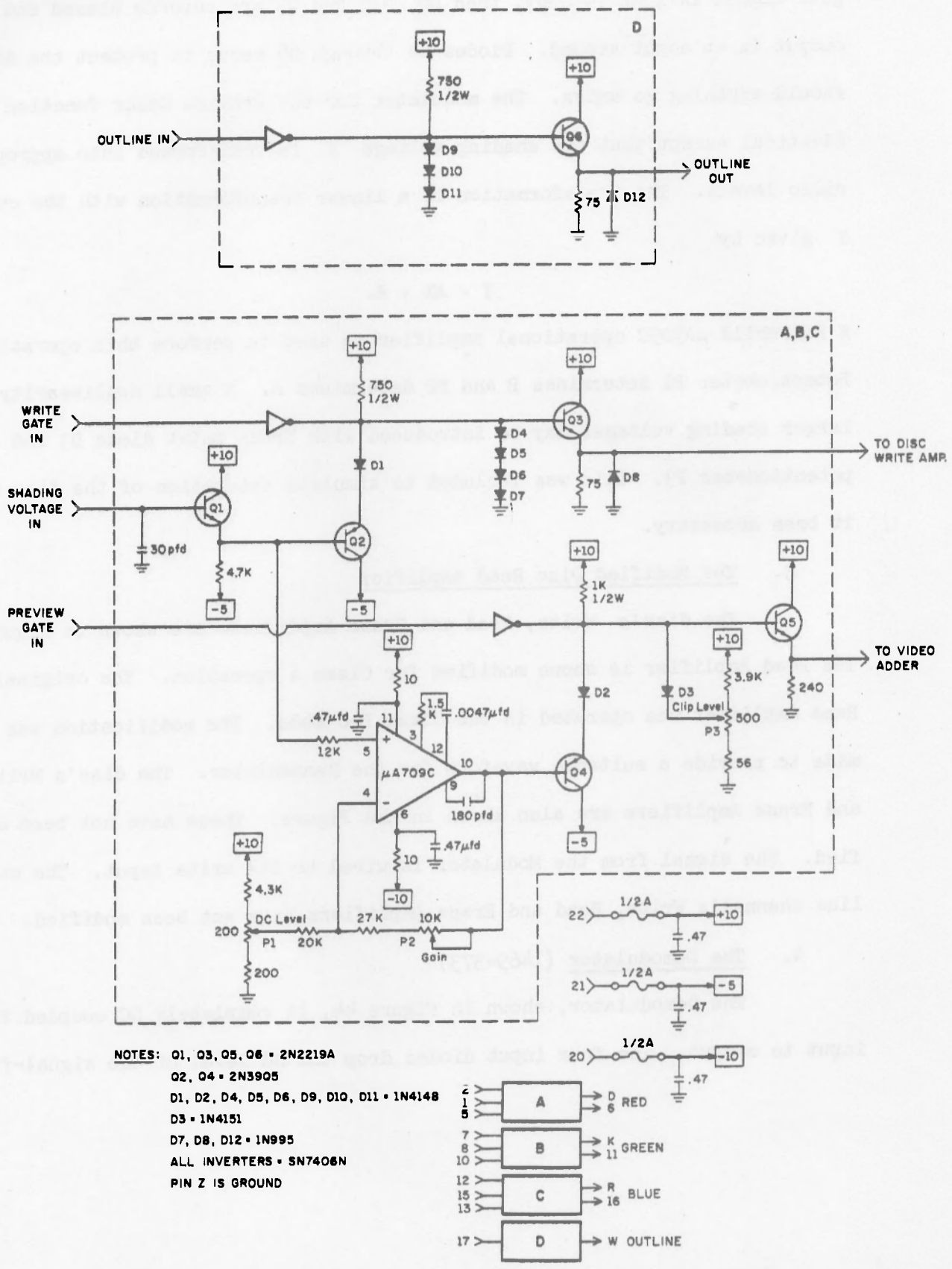


Figure 42. The Modulator (A, B, C) and L/V Converter (D)

gate signal is high (~ GND), then Q2, D1, and Q3 are reverse biased and the output is at about ground. Diodes D4 through D8 serve to protect the disc should anything go amiss. The modulator for the Preview Color function is identical except that the shading voltage X is transformed into appropriate video levels. The transformation is a linear transformation with the output Y given by

$$Y = AX + B.$$

A Fairchild μA709C operational amplifier is used to perform this operation. Potentiometer P1 determines B and P2 determines A. A small nonlinearity for larger shading voltages may be introduced with break point diode D3 and potentiometer P3. This was included to simulate saturation of the disc had it been necessary.

3. The Modified Disc Read Amplifier

The disc's Write, Read and Erase Amplifiers are shown in Figure 43. The Read Amplifier is shown modified for Class A operation. The original Read Amplifier was operated in the Class B-C mode. The modification was made to provide a suitable waveform for the Demodulator. The disc's Write and Erase Amplifiers are also shown in the Figure. These have not been modified. The signal from the Modulator is wired to the write input. The outline channel's Write, Read and Erase Amplifiers have not been modified.

4. The Demodulator (1469-373)

The Demodulator, shown in Figure 44, is completely DC coupled from input to output. The four input diodes drop the DC level of the signal from

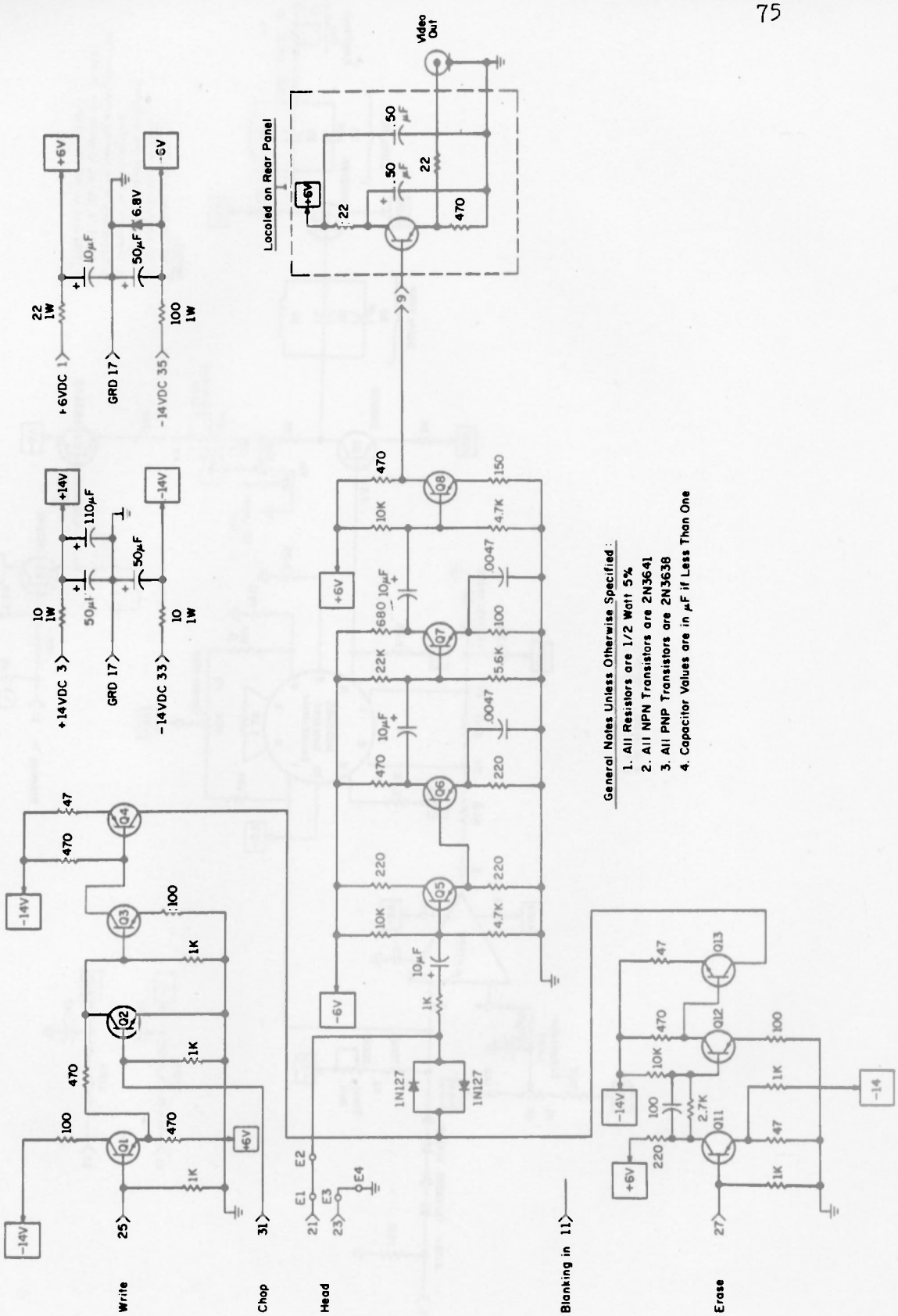


Figure 43. Modified Disc Amplifier

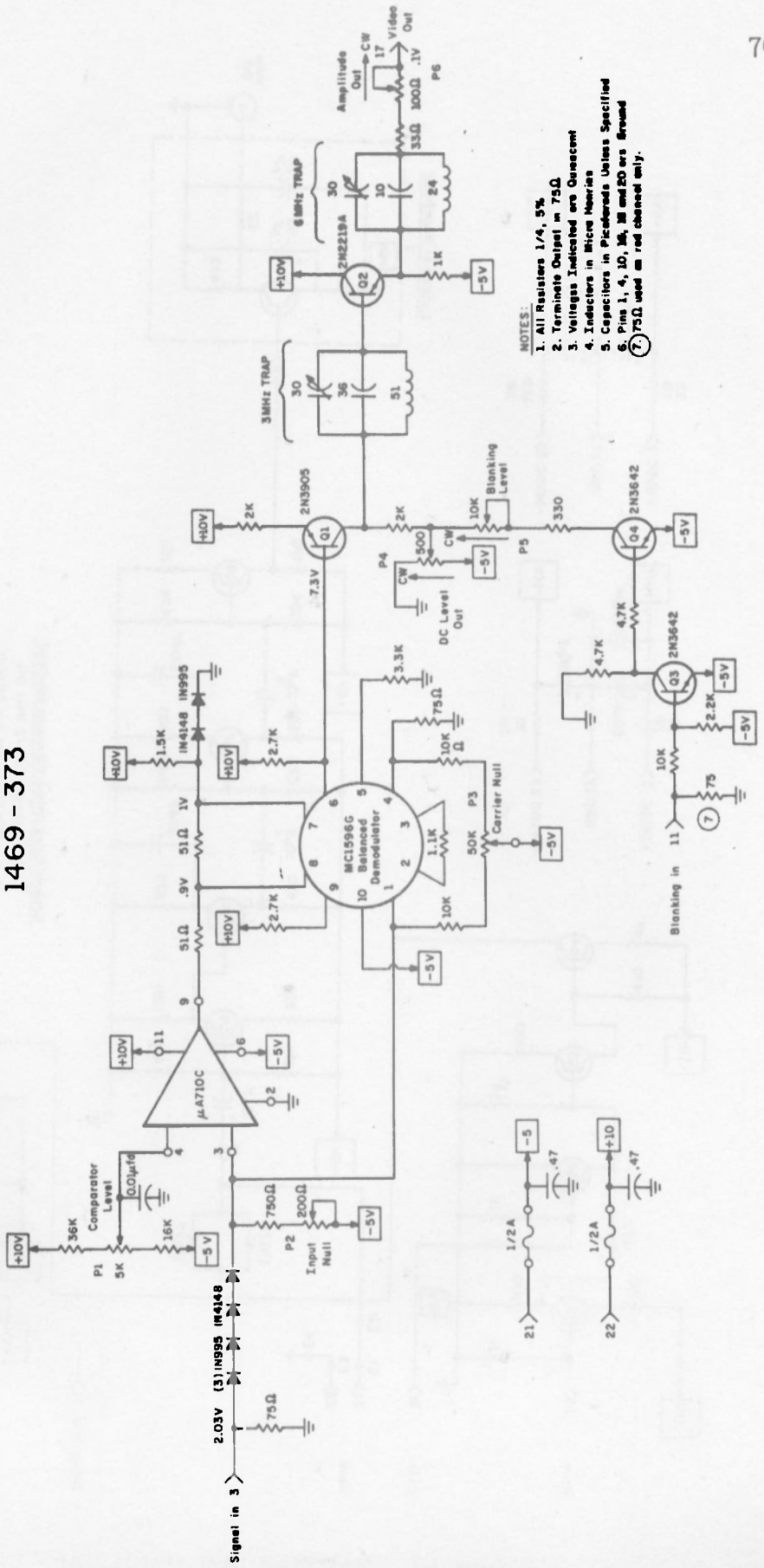


Figure 44. The Demodulator

2.03 volts to ground. The level may be made very close to ground by properly adjusting P2. The carrier signal is derived from the signal itself in order to obtain a high quality demodulation for both color areas and color points, as well as to compensate for disc drifts. The color areas are modulated at about 3 MHz while the color points are chopped at a higher frequency. The disc is synchronized to the 60 Hz line and this causes drifts in the disc speed as the line frequency changes. With the disc's speed varying in time, it would be very hard to use an external source for the carrier signal. A Fairchild μA710C comparator is used to provide the carrier signal to a Motorola MC1596G balanced demodulator integrated circuit. This integrated circuit effectively forms the product of the input signal, $f(t)\cos\omega_c t$ and the carrier signal, $\text{sign}[\cos\omega_c t]$. Disregarding the DC level, and for small delays, the output is proportional to

$$f(t)\cos(\omega_c t)\text{sign}[\cos\omega_c t].$$

If we break $\text{sign}[\cos\omega_c t]$ into its Fourier components, we have

$$\text{sign}[\cos\omega_c t] = \frac{4}{\pi}\left[\cos\omega_c t - \frac{1}{3}\cos 3\omega_c t + \frac{1}{5}\cos 5\omega_c t + \ldots\right].$$

The expression for the product then becomes [29]

$$f(t)\cos(\omega_c t)\text{sign}[\cos\omega_c t] =$$

$$\frac{2}{\pi} f(t) + \frac{4f(t)}{3\pi}\cos(2\omega_c t) - \frac{4f(t)}{15\pi}\cos(4\omega_c t) + \ldots \qquad (1)$$

which depends only on $f(t)$ and even multiples of the chopping frequency ω_c. The output from the balanced demodulator is at a collector level DC voltage and the signal polarity is opposite to that desired. Transistor Q1 inverts the signal and shifts the DC level. Two LC parallel traps are used to suppress harmonics of the modulation frequency. The expansion (1) above shows that if filters at $2\omega_c$, $4\omega_c$, ... are used then the final output will be

proportional to f(t). Theoretically, then, traps set at $2\omega_c$ and $4\omega_c$ would give us the best result. Experimentally, it was found that a trap at ω_c was needed. This trap attenuates residual chopping frequency components that slip through the Demodulator because of the carrier delay and feedthrough. The trap set at $2\omega_c$ (~6MHz) removes about 80% of the ripple while the one set at ω_c (~3MHz) removes only ~5%. A photograph of a sample input signal and the corresponding output is shown in Figure 45. Potentiometer P4 sets the output DC level, P5 sets the blanking level and P6 adjusts the amplitude. The carrier null potentiometer P3 should be adjusted for a minimum of 3 MHz feedthrough when the 3 MHz trap is detuned.

5. The Video Adder (1469-180B)

The 8-input Video Adder, shown in Figure 46, is the same basic circuit as the 3-input Video Adder used in the ATC - Mark I [1], except with 8 inputs. Only 6 of these inputs are used in the ATC - Mark II. This completes the discussion of the circuitry added to the ATC - Mark I to form the ATC - Mark II.

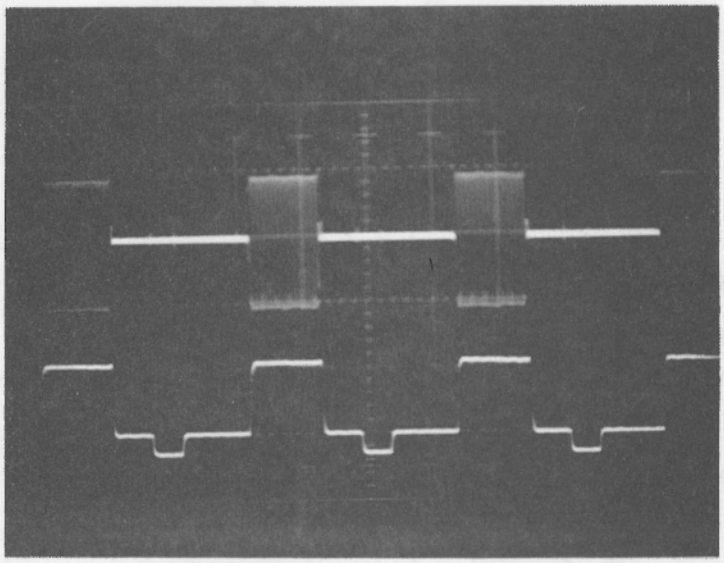


Figure 45. Demodulator Waveforms

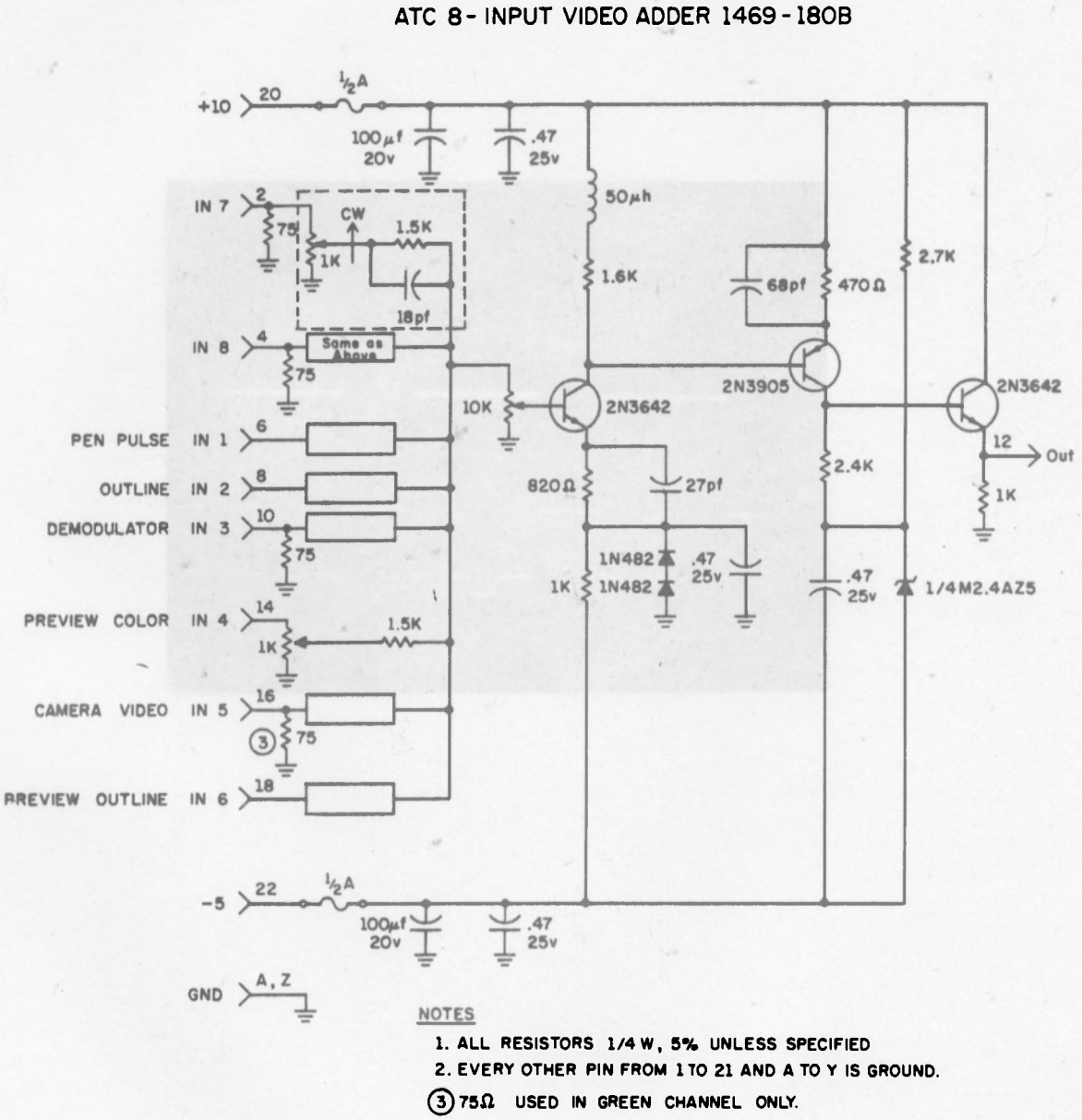


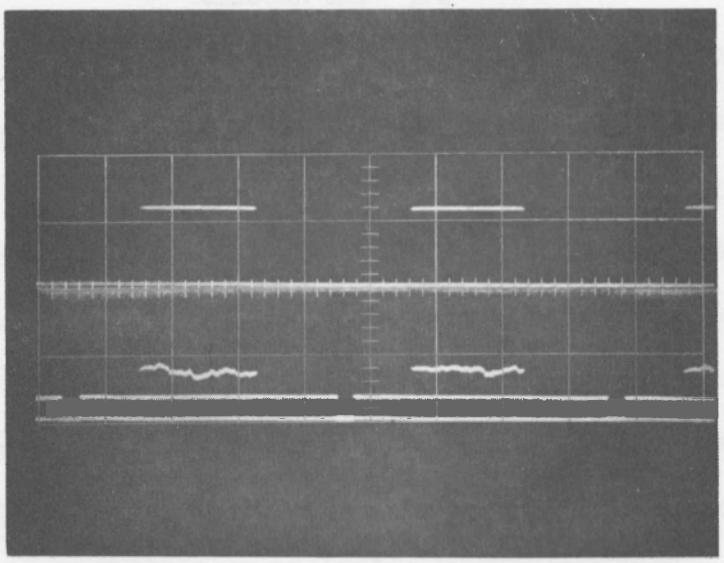
Figure 46. Video Adder

IV. THE RESULTS

The ATC - Mark II as described here has been assembled and is working. It incorporates all of the features of the ATC - Mark I. The quality of the display has been upgraded, eliminating the vertical color bars. In addition, the machine is capable of coloring different shades which are selected by the operator using the shading potentiometers. The shade may be selected using a "preview color area" displayed on the CRT face, or the adventuresome operator may continuously vary the shade during the coloring process until he finds the one he wants. With the light pen in the "WRITE" mode, points appearing on the screen may be varied in intensity as they are written.

One difficulty encountered during this investigation affects the quality of the result of the shading circuitry. The top photo in Figure 47 shows storage scope waveforms for the input write signal and the resulting signal out of the Demodulator. The viewing time shown is about one frame. We see that somewhere between the input and the output, a distortion takes place. The bottom photo shows the input and output waveforms of the Demodulator. We see that the unusual modulation is coming from the disc surface. Although these variations are quite visible on the display, nothing has been done here to correct the result. It is believed that this modulation arises from a non-uniform magnetic coating on the disc. Newer video discs use FM modulation schemes to avoid this problem. Other than this problem, all of the goals for the shading circuitry have been attained.

The ATC - Mark II has been designed so that if the machine is going to be used in a situation in which the camera input becomes unnecessary, the camera may be safely removed. If, however, the camera input is necessary, the operator may switch between the several options that are available to



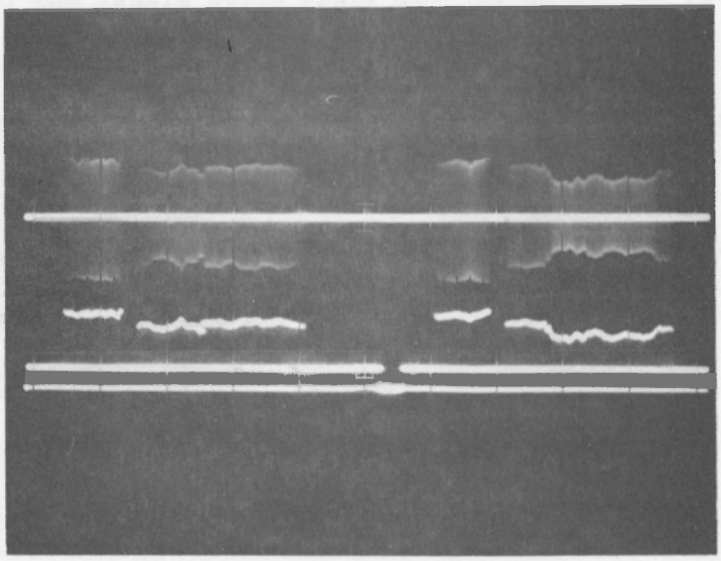
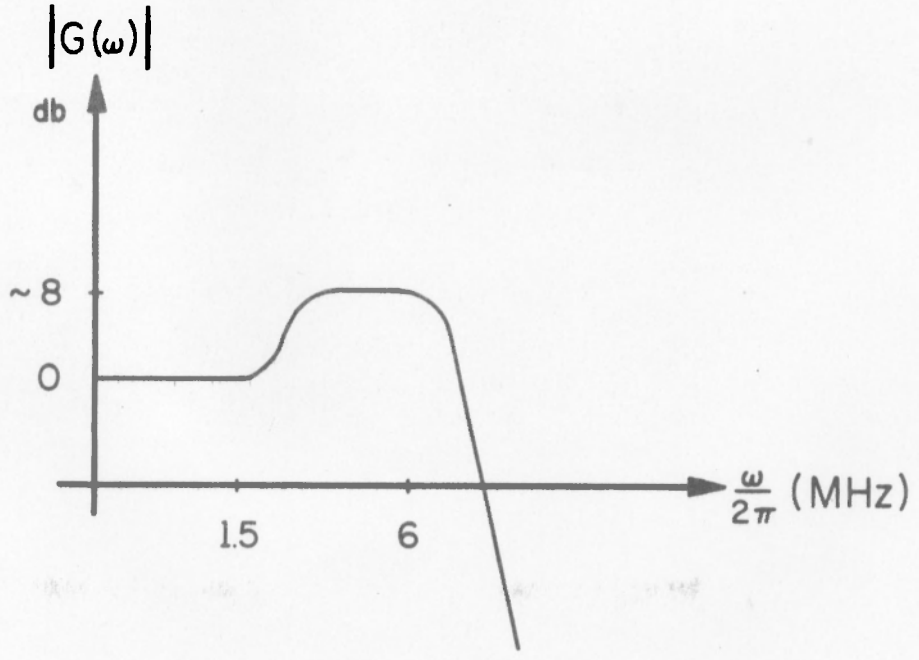


Figure 47. Disc Problems

him by using the Switch Card. The outline may be previewed by pushing the "PREVIEW OUTLINE" button. This allows the operator to set up the exact scene as he wants it. The outline may then be stored on the disc by pushing the "STORE OUTLINE" button. After storage, the outline may be colored in as desired. In actual practice, the outlining circuitry has proved to be only marginally useful for most operators. The reason for this is that most people prefer to draw their own outlines directly on the television screen. The use of this secondary source of input does not interest most people. Regardless of this, all of the basic goals for the outlining circuitry have been met.

Comments on selected circuits:

(1) The Horizontal Delay Line Differentiator circuit and Logic should be improved. The design is basically correct, but it suffers from noise problems. Something to try would be to put an active filter in before amplifying that would have a gain $G(\omega)$ something like that in the graph below.



The use of such a band peaking amplifier would likely be to increase the effect of the high frequency components and the resolution. This might peak the useful signal that appears to be noise with the present arrangement.

The arrangement of the double-line correction one-shots should also be changed. Rather than trigger a one-shot on the negative portion of the signal, delaying the original, ORing the delayed and one-shotted signal and then one-shotting the result, a more efficient circuit would result by one-shotting on the leading edge of the signal, ORing the one-shotted signal and the real-time signal and then one-shotting the result. This would do the same thing far more economically.

(2) Another problem remaining is that the Vertical Differentiation Circuit requires a long warm-up time. It is believed that this is due to the AGC diodes in the Corning delay line. The problem would probably disappear if these diodes were replaced with an appropriate resistor.

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APPENDIX A.

THE DELAY LINE DIFFERENTIATION SCHEME

For a continuous function f(t), the derivative $f'(t)$ may be written as:

$$f'(t) = \lim_{T \to 0} \frac{f(t) - f(t-T)}{T}$$

The following describes the use of a shorted delay line to approximate the derivative by forming the difference

$$\Delta f(t) = f(t) - f(t-2T).$$

This differentiation scheme is discussed in References [19] and [20].

1. The Delay Line [19], [21], [22], [23], [24]

The lumped constant delay line used here has a 125 MHz cutoff frequency, a 90Ω impedance, and a maximum DC resistance of 4.5Ω for its 100 ns length. If the Fourier spectrum of the delay line input signal is mainly composed of frequencies much less than the line's cutoff frequency, then the characteristic impedance Z_0 becomes a real constant and the phase factor β becomes strictly proportional to frequency. These approximations may be made when $1 - \left(\frac{f}{f_c}\right)^2 \sim 1$ where f_c is the cutoff frequency, and f is the frequency of operation. The camera's video amplifier 3db bandwidth is 7 MHz so that the video's Fourier spectrum should be small for frequencies greater than about 10 MHz. With $f \leq 10$ MHz, $1 - \left(\frac{f}{f_c}\right)^2 \geq 0.9936$ and the approximations are applicable. For $f < f_c$, the attenuation is due to the DC resistance of the line. The attenuation in percent is:

$$\text{Attenuation}(\%) = \frac{R_{DC}}{Z_0 + R_{DC}} \times 100\%,$$

and the delay line output is multiplied by a factor

$$a = 1 - \frac{\text{attenuation } (\%)}{100}.$$

For a 160 nsec round trip delay, $R_{DC} \sim 7$ ohms and $a \sim .93$.

2. The Model for Analysis

The ideal delay line model will be used here over the entire frequency range from minus infinity to infinity for purposes of analysis. This may be done because the actual delay line behaves much like an ideal delay line over the range of frequencies that the video signal's Fourier spectrum takes on. For purposesof analysis, then, the model's transfer function becomes

$$G(\omega) = e^{-i\omega T}. \quad -\infty < \omega < \infty$$

The characteristic impedance Z_0 becomes a constant for all ω.

3. The Impulse Response [25], [26], [28], [29]

One way of determining the response $r(t)$ of a network to a waveform $w(t)$ is to find the response $g(t)$ of the network to the impulse function $\delta(t)$ and convolve it with $w(t)$. In equation form $r(t) = w(t)*g(t)$. The impulse response $g(t)$ can be obtained in many cases through a Fourier transform analysis. The Fourier transform pair that will be used here is:

$$\mathcal{F}[f(t)] = F(\omega) = \int_{-\infty}^{\infty} f(t)e^{-i\omega t}dt$$

and

$$\mathcal{F}^{-1}[F(\omega)] = f(t) = \frac{1}{2\pi}\int_{-\infty}^{\infty} F(\omega)\, e^{+i\omega t}d\omega$$

If $G(\omega)$ is the transfer function of the network, then the impulse response $g(t)$ is given by

$$g(t) = \mathcal{F}^{-1}[1 \cdot G(\omega)]$$

$$= \mathcal{F}^{-1}[G(\omega)]$$

because the Fourier transform of $\delta(t)$ is 1.

For the ideal delay line, we find

$$g(t) = \delta(t-T)$$

and the response of the network to an arbitrary waveform $w(t)$ is just

$$r(t) = w(t)*g(t) = w(t)*\delta(t-T) = w(t-T)$$

as might be expected.

4. The Circuit

The top drawing in Figure 48 shows the delay line differentiator circuit with an input f and output v_o. The resistor R_1 provides an impedance match to Z_0 at the driving end of the circuit to give a reflection coefficient close to zero. The computation of v_o for any f is complicated to do directly because the input impedance of the line is a complicated function of time. For a line operating without overlapping reflections, the input impedance of the line is the characteristic resistance of the line Z_0. If the line is initially uncharged, then the computation of v_o is considerably simplified by using the impulse response approach because interference effects need not be accounted for. The bottom drawing in Figure 48 shows the delay line circuit with an impulse voltage δ input and the impulse response g at the output. The input voltage impulse δ shown will suffer an attenuation due to the resistive divider R_1 and Z_0 giving an effective input impulse for computation of g(t) by

$$\frac{Z_0}{R_1 + Z_0}\delta(t)$$

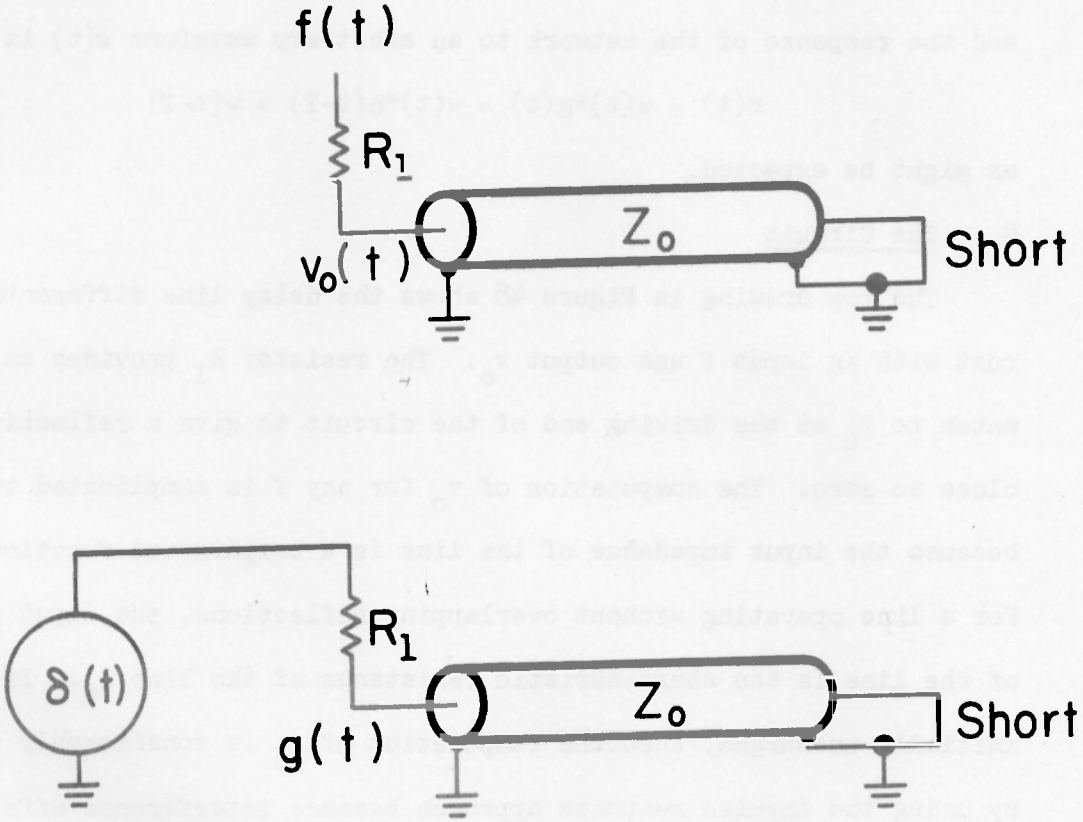


Figure 48. Delay Line Circuit

This impulse then travels down the line for a time T before encountering a short circuit with a voltage reflection coefficient ρ of minus one. When the impulse reappears at the sending end of the delay line, it has suffered a sign reversal with a total round trip attenuation a and delay 2T. No further reflections take place if $R_1 = Z_0$. The delay line's reflected response to $\frac{Z_0}{R_1 + Z_0}\delta(t) = g_1(t)$ is then

$$g_2(t) = \frac{Z_0}{R_1 + Z_0}\rho a\delta(t-2T).$$

The total impulse response g(t) is the superposition of $g_1(t)$ with the reflected impulse $g_2(t)$ giving

$$g(t) = g_1(t) + g_2(t) =$$

$$= \frac{Z_0}{R_1 + Z_0}[\delta(t) + \rho a\delta(t-2T)] =$$

$$= \frac{Z_0}{R_1 + Z_0}[\delta(t) - a\delta(t-2T)].$$

The output $v_o(t)$ for a general input f(t) will then be given by

$$v_o(t) = f(t)*g(t) =$$

$$= \frac{Z_0}{R_1 + Z_0}[f(t)*\delta(t) - af(t)*\delta(t-2T)] =$$

$$= \frac{Z_0}{R_1 + Z_0}[f(t) - af(t-2T)],$$

which is just the result one might expect.

5. Corrected Difference

Although the preceding analysis was symbolic, it reaffirms our hypothesis that a shorted delay line accurately forms the difference of two signals. The only snag remaining is the attenuation a. If we subtract $v_o(t)$ from

$\frac{Z_0}{R_1 + Z_0}$ (1-a)f(t), the result $v_c(t)$ is

$$v_c(t) = -a \frac{Z_0}{R_1 + Z_0} [f(t) - f(t-2T)] .$$

We see that this manipulation effectively removes the unbalancing effect of the attenuation.

6. The Region of Approximation

Let us define

$$\Delta f = f(t) - f(t-2T) .$$

The Fourier transform of Δf is:

$$\Delta F = \mathcal{F}[\Delta f] = (1-e^{-i\omega 2T})F(\omega) = D(\omega)F(\omega)$$

where $D(\omega) = 1-e^{-i\omega 2T}$. This function is plotted on the complex plane in Figure 49(a). Rewriting, we find

$$D(\omega) = e^{-i\omega T}(e^{i\omega T} - e^{-i\omega T}) = 2ie^{-i\omega T}\sin\omega T =$$

$$= 2\sin(\omega T)e^{i(\frac{\pi}{2} - \omega T)} .$$

The magnitude and phase of $D(\omega)$ are seen to be

$$|D(\omega)| = 2\sin\omega T$$

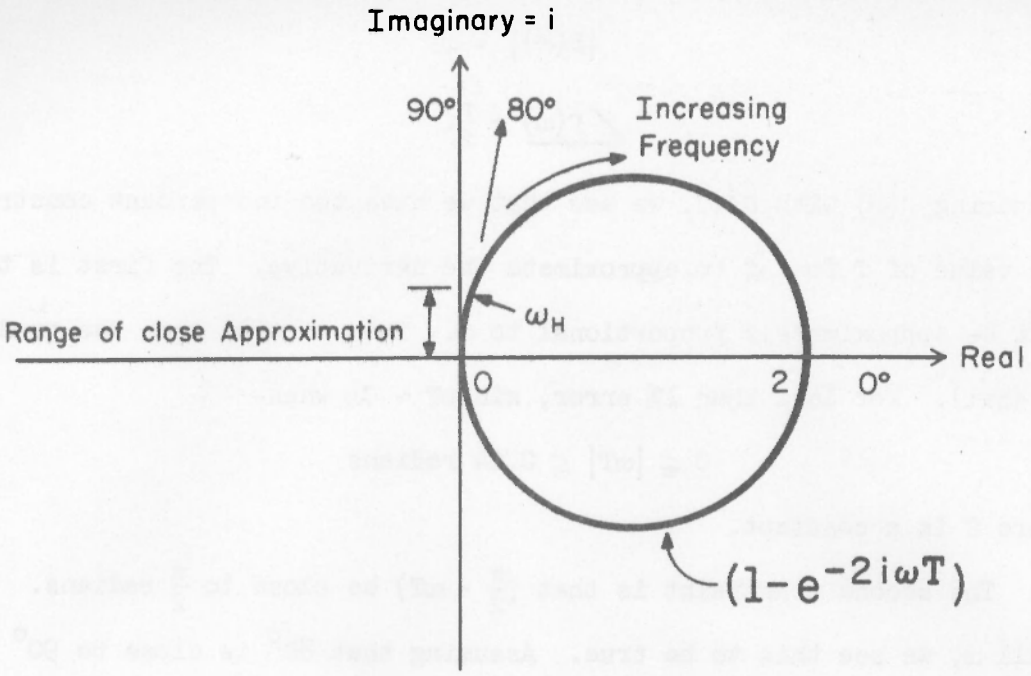
and

$$\angle D(\omega) = \frac{\pi}{2} - \omega T .$$

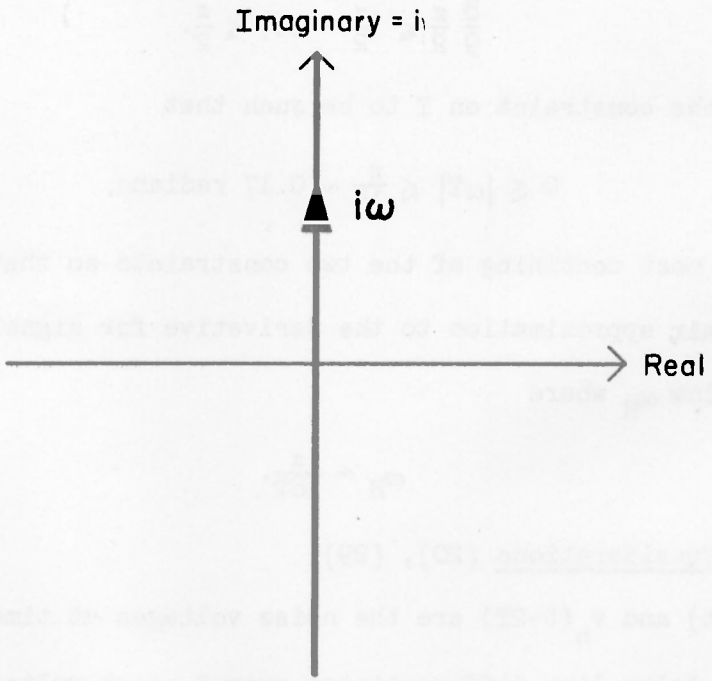
We need to compare these results with those for the Fourier transform of the derivative $f'(t)$. The transform is:

$$\mathcal{F}[f'(t)] = i\omega F(\omega) = \Gamma(\omega)F(\omega)$$

where $\Gamma(\omega) = i\omega = \omega e^{i\frac{\pi}{2}}$. This function is plotted on the complex plane in Figure 49(b). The magnitude and phase of $\Gamma(\omega)$ are seen to be



(a) Plot of $1-e^{-i\omega 2T}$



(b) Plot of iω

Figure 49. iω Compared with $1-e^{-i\omega 2T}$

$$|\Gamma(\omega)| = \omega$$

and

$$\angle \Gamma(\omega) = \frac{\pi}{2}.$$

Comparing $\Gamma(\omega)$ with $D(\omega)$, we see that we have two independent constraints on the value of T for Δf to approximate the derivative. The first is that $\sin\omega T$ must be approximately proportional to ω. This is true when the product ωT is small. For less than 1% error, $\sin \omega T \sim C\omega$ when

$$0 \leq |\omega T| \leq 0.24 \text{ radians}$$

where C is a constant.

The second constraint is that $(\frac{\pi}{2} - \omega T)$ be close to $\frac{\pi}{2}$ radians. For small ω, we see this to be true. Assuming that 80° is close to 90° for our purpose, we have,

$$\frac{8}{9}\frac{\pi}{2} \leq (\frac{\pi}{2} - \omega T) \leq \frac{\pi}{2}.$$

This gives the constraint on T to be such that

$$0 \leq |\omega T| \leq \frac{\pi}{18} \sim 0.17 \text{ radians.}$$

This is the most confining of the two constraints so that the shorted delay line is a fair approximation to the derivative for signals composed of frequencies below ω_H where

$$\omega_H \sim \frac{\pi}{18T}.$$

7. Noise Considerations [20], [29]

If $v_n(t)$ and $v_n(t-2T)$ are the noise voltages at times t and t-2T respectively, the delay line differentiator output noise voltage $v_{n_o}(t)$ is given by

$$v_{n_o}(t) - v_n(t) - v_n(t-2T).$$

If we assume that $v_n(t)$ and $v_n(t-2T)$ are uncorrelated and that the noise is uniformly distributed in time, then the r.m.s. noise voltage E_n at time t is

the same as that at any other time. The resulting r.m.s. noise voltage at the output E_{n_o} is

$$E_{n_o} = \sqrt{E_n^2 + E_n^2} = \sqrt{2}E_n.$$

We see then, that the delay line differentiation scheme increases the r.m.s. noise voltage by a factor of $\sqrt{2}$. Assuming that $|\omega T|$ is small, ΔF can be written as

$$\Delta F = (1-e^{-i\omega 2T})F(\omega) \sim i\omega 2TF(\omega).$$

Fourier-transforming this result, we see that

$$\Delta f \sim 2Tf'(t).$$

As T is decreased, we see that Δf will decrease. As T further decreases, a point will be reached where the r.m.s. value of the noise E_{n_o} is comparable to the r.m.s. value of the signal, E_{s_o}. Thus, a further constraint on the system is that T be large enough to make

$$E_{s_o} \gg E_{n_o} = \sqrt{2}E_n.$$

For large video S/N ratios, it is feasible to use the delay line differentiation scheme.

APPENDIX B.

THE ONE FRAME GATE DESIGN

The circuit and notation for the one frame gate is shown in Figure 40 of the text. The Moore circuit design (pulse input - level output) technique will be used here. The design diagrams are shown in Figure 50(a) through (f). The timing diagram is given in (g). A LVD pulse occurs once per field so that two such pulses must be spanned to form a one frame gate. The state transition diagram for a one frame gate is shown in (a). The corresponding state transition table is given in (b). If we assign states using adjacent Gray code, a suitable assignment is:

$$a = 00 \quad b = 01 \quad c = 11 \quad d = 10.$$

For this assignment, the state transition table with state assignment is as shown in (c). From this table we see that $GO = q_1$. The state transition table for q_1 is given in (d) and that for q_2 is given in (e). The SO signal is used to set the flip-flop output to one with the preset input, PR.

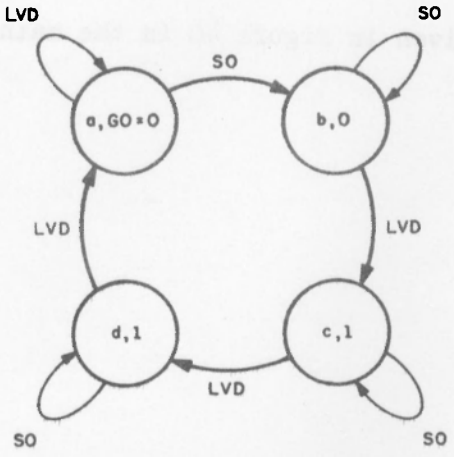
We have

$$PR_n = \begin{cases} q_n^{\nu+1} & \text{when } q_n^{\nu} = 0 \\ d & \text{when } q_n^{\nu} = 1 \end{cases}$$

where d stands for the "don't care" action. The "don't care" is used because if the flip-flop output is already one, then presetting it won't have any effect. For D-type flip-flops, the next state is the present state of the D input. In equation form

$$D_n = q_n^{\nu+1}.$$

The clock for the D inputs is Logical Vertical Drive (LVD).



SO : Store Outline
LVD : Logical Vertical Drive
GO : Gate Outline

(a)

$Q^{\nu+1}$

Q^{ν}	SO	LVD	GO
a	b	a	0
b	b	c	0
c	c	d	1
d	d	a	1

(b)

$q_1^{\nu+1}\, q_2^{\nu+1}$

$q_1^{\nu} q_2^{\nu}$	SO	LVD	GO
00	01	00	0
01	01	11	0
11	11	10	1
10	10	00	1

(c)

$q_1^{\nu+1}$

$q_1^{\nu} q_2^{\nu}$	SO	LVD
00	0	0
01	0	1
11	1	1
10	1	0

(d)

$q_2^{\nu+1}$

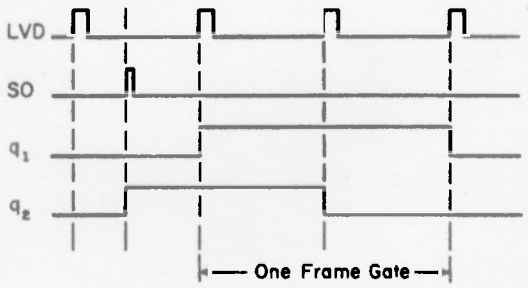
$q_1^{\nu} q_2^{\nu}$	SO	LVD
00	1	0
01	1	1
11	1	0
10	0	0

(e)

	SO		SO
00	0	00	1
01	0	01	d
PR_1 11	d	PR_2 11	d
10	d	10	0

	LVD		LVD
00	0	00	0
01	1	01	1
D_1 11	1	D_2 11	0
10	0	10	0

(f)



(g)

Figure 50. One Frame Gate Design Diagrams

Using these rules, we obtain the flip-flop excitation maps shown in (f). From these we obtain expressions for the flip-flop preset and D inputs:

$$PR_1 = 0 \qquad D_1 = q_2$$

$$PR_2 = \bar{q}_1 \cdot SO \qquad D_2 = \bar{q}_1 q_2 .$$

The implementation of this design is given in Figure 40 in the main body of this thesis.

APPENDIX C.

CARD RACK LISTS

1. CARD RACK A

1. Switch Matrix
2. Indicator
3. Total Erase Control
4. Logic to Video Converter
5. Brightness Control
6. 2-Input Nand
7. 2-Input Nand
8. +1 Volt Generator/Mode Switch
9. 3-Input Nand
10. Modulator; L/V Converter
11.
12.
13. 2-Input Nand
14. One-Frame Gate
15. Pen Pulse Shaping Circuit
16. Video Gate; L/V Converter
17. Video to Logic Converter
18.
19. 8-Input Video Adder
20. 8-Input Video Adder
21. 8-Input Video Adder
22.
23. Demodulator
24.
25. Demodulator
26.
27. Demodulator
28.

2. CARD RACK B

1. Level Shifter
2. Horizontal Oscillator
3. Horizontal Counter
4. Horizontal Buffer
5. 9-Bit Register and Coincidence
6. 2-Input Nand
7. Dual 9-Bit Register
8. 9-Bit Register and Coincidence
9. 2-Input Nand
10. 9-Bit Register and Coincidence
11. 9-Bit Register and Coincidence
12. 2-Input Nand
13. LVD, LHD Distribution Buffer
14. Vertical Counter
15. Vertical Buffer
16. 8-Bit Register and Coincidence
17. 2-Input Nand
18. 8-Bit Register and Coincidence
19. 8-Bit Register and Coincidence
20. 8-Bit Register and Coincidence
21.
22.
23.

.
.
.

28.

3. CARD RACK C

1. One-Shot Buffer
2. 4-Input Nand
3. 2-Input Nand
4. 3-Input Nand
5. R-S Flip-Flop and 2-Bit Coincidence
6. Indicator
7. R-S Flip-Flop
8. 2-Input Nand
9. 2-Input Nand
10. 3-Input Nand
11. J-K Flip-Flop
12.
13. PC Area; Logical Blanking
14. Synchronous Chopper
15. Vertical Differentiator Logic
16. Vertical Differentiator
17.
18. Video Distribution Amplifier
19. Delay One-Shot and Switch Shifters
20. RC Filter Differentiator
21. Horizontal Differentiator Logic
22. Horizontal Delay Line Differentiator
23.
24. Switch Card
25.
26.
27. ±12 Volt Power Supply
28.

APPENDIX D.

PHOTOGRAPHS OF THE OUTLINING SCHEME

Photographs illustrating the performance of the outlining scheme are shown here. Figure 51 illustrates the performance for a line drawing and Figure 52 illustrates the performance for a solid area. It is interesting to note in each of these sets of photos that the HLD (Horizontal Logical Derivative) is missing the horizontal parts and that the VLD (Vertical Logical Derivative) is missing the vertical parts with both the HLD and the VLD containing the parts that are skewed. The LD (Logical Derivative) shown is given by

$$LD = HLD \vee VLD$$

where $\vee$ stands for "OR" so that the final outline is an "all-direction" outline.

It should be noted that the outline control switches are in different positions for each figure. For any line drawing, there is a set of switch positions that will "optimize" the LD. For different line drawings, the switch positions may be different depending on how nice an outline is wanted. In some cases, the comparator potentiometers may have to be adjusted.

As discussed in Chapter II, for scenes composed of both solid areas and line drawing areas (see Figure 6), a correction scheme has been implemented. The pictures shown in Figure 53 illustrate what happens when the correction scheme is not used (a) and when it is (b). The result in (a) for the original line drawing is double lines. The result in (b) for the same original is discontinuities in the HLD. As there is no correction circuit for the VLD, horizontal lines would appear doubled if they had been shown. The

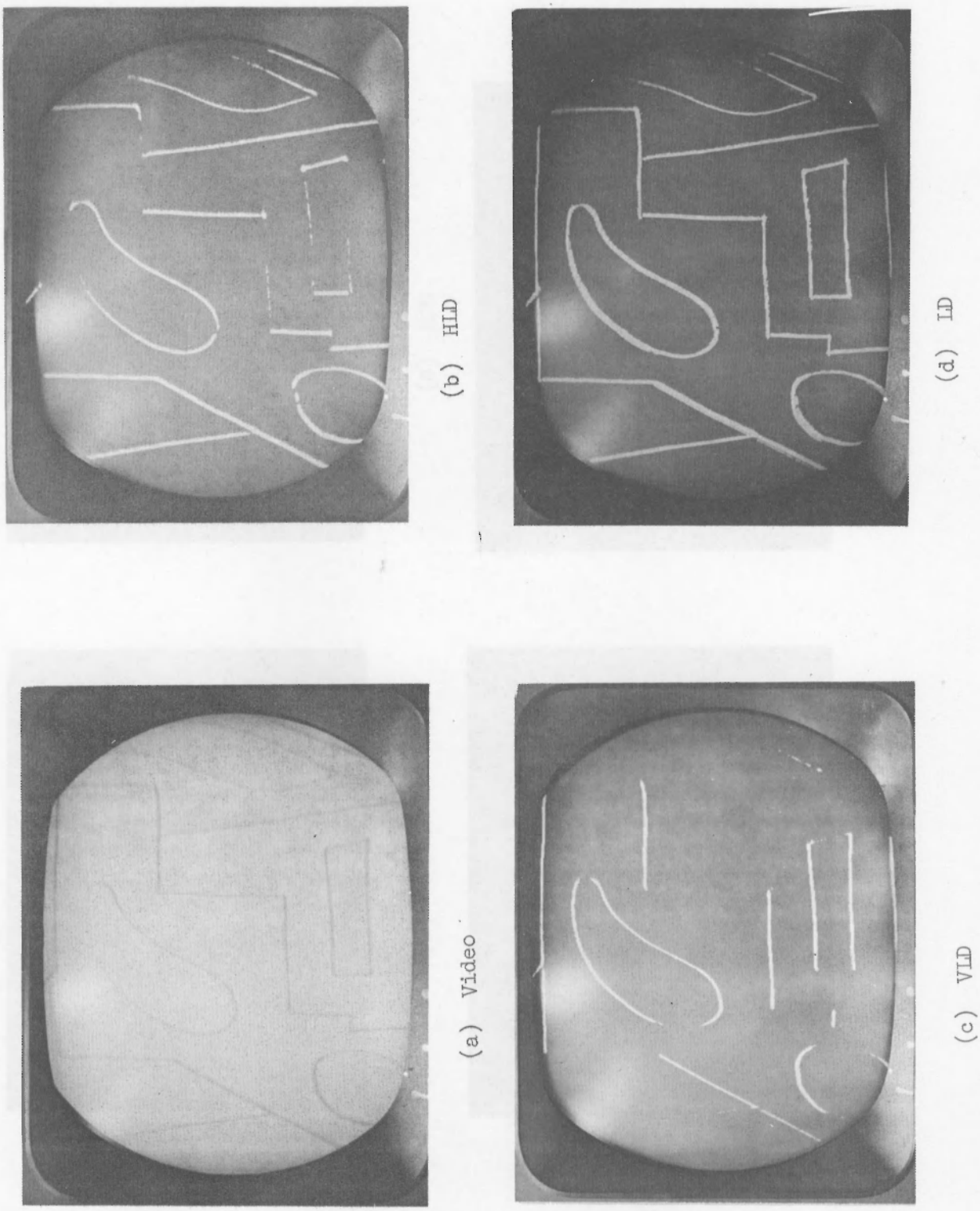


Figure 51. Performance for a Line Drawing

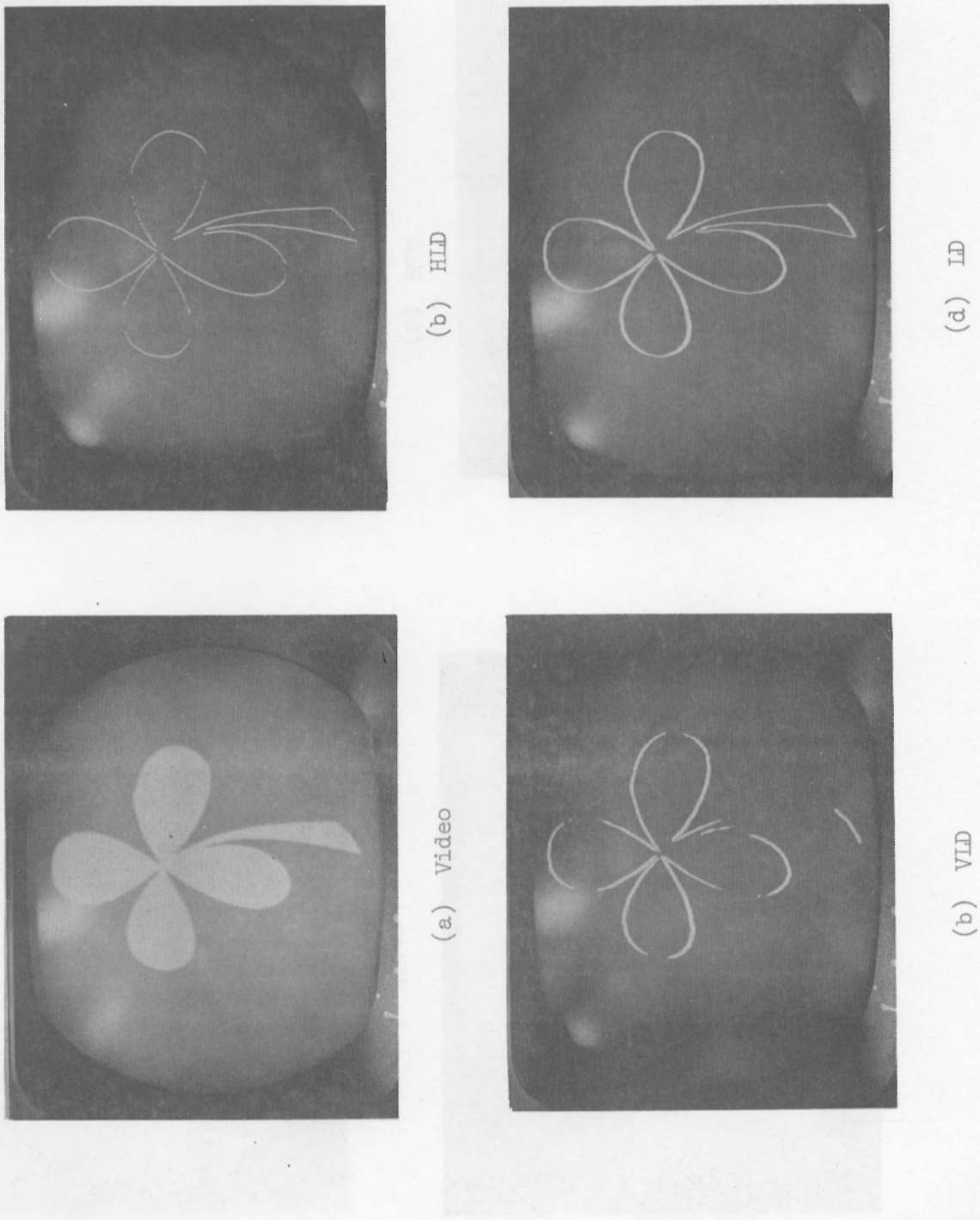
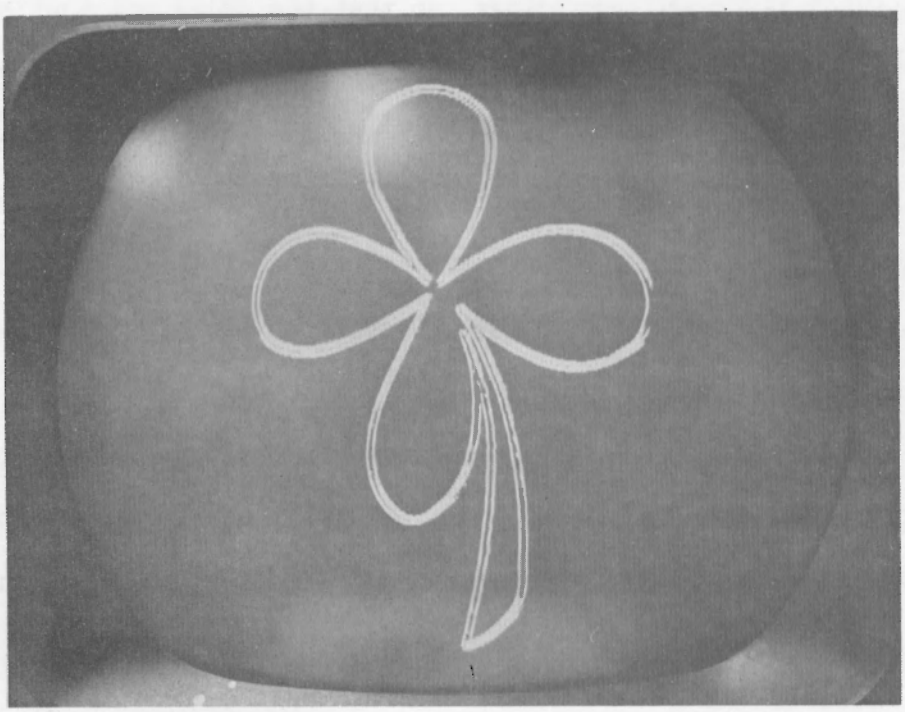
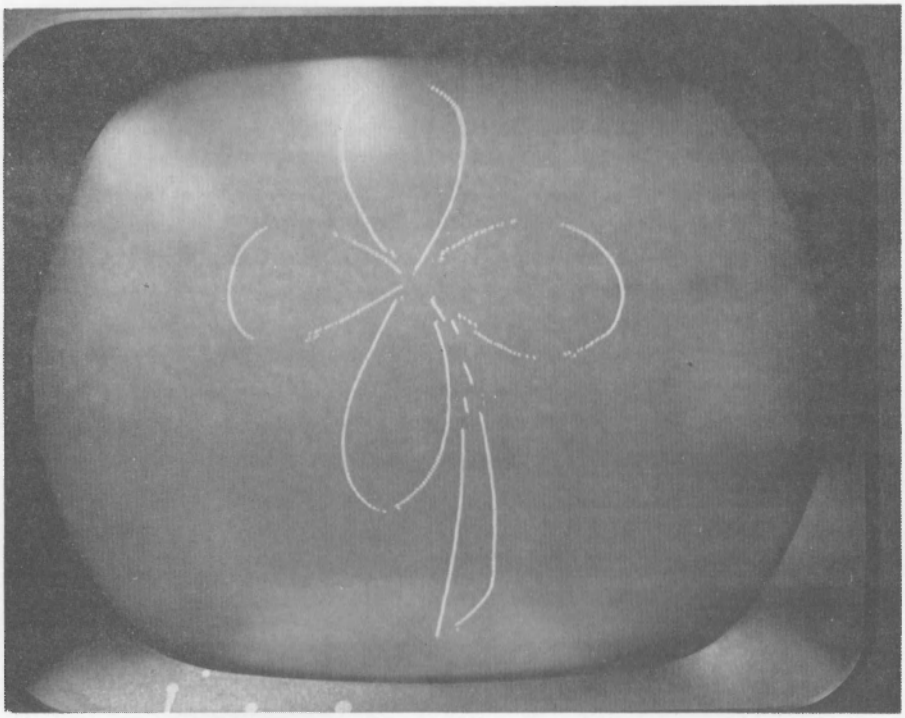


Figure 52. Performance for a Solid Area



(a) LD without Correction



(b) HLD with Correction

Figure 53. Double Line Correction

discontinuities shown in the stem of the four leaf clover occur where two vertical lines are very close, so that the delay one-shot wipes out the second of the two lines. The zig-zag effect in the stem occurs when the leading edge of the stem was overlapped by the one-shot but the trailing edge was not. There are also discontinuities where there should be cusps. For scenes composed exclusively of solid areas or of line drawings, other switch settings will result in a better job of outlining, as was shown in Figures 51 and 52.

It is interesting to apply the outlining circuitry to photographs. This is shown in Figure 54. The outlining scheme may be applied to moving scenes without difficulty because all circuitry operates in "real time".

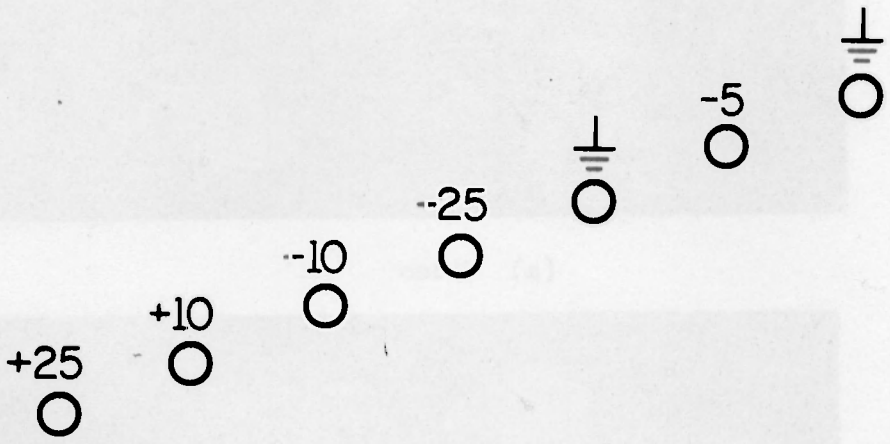
(a) Video

(b) LD

Figure 54. The LD for a Photograph

APPENDIX E.

POWER SUPPLY BUSS BARS



APPENDIX F.

PHOTOGRAPH DISPLAYING THE COLORING CAPABILITY

Figure 55 shows a sample of artwork that was generated with the ATC - Mark II. Color photographs of the ATC - Mark I were published in the November/December 1969 issue of Information Display magazine.

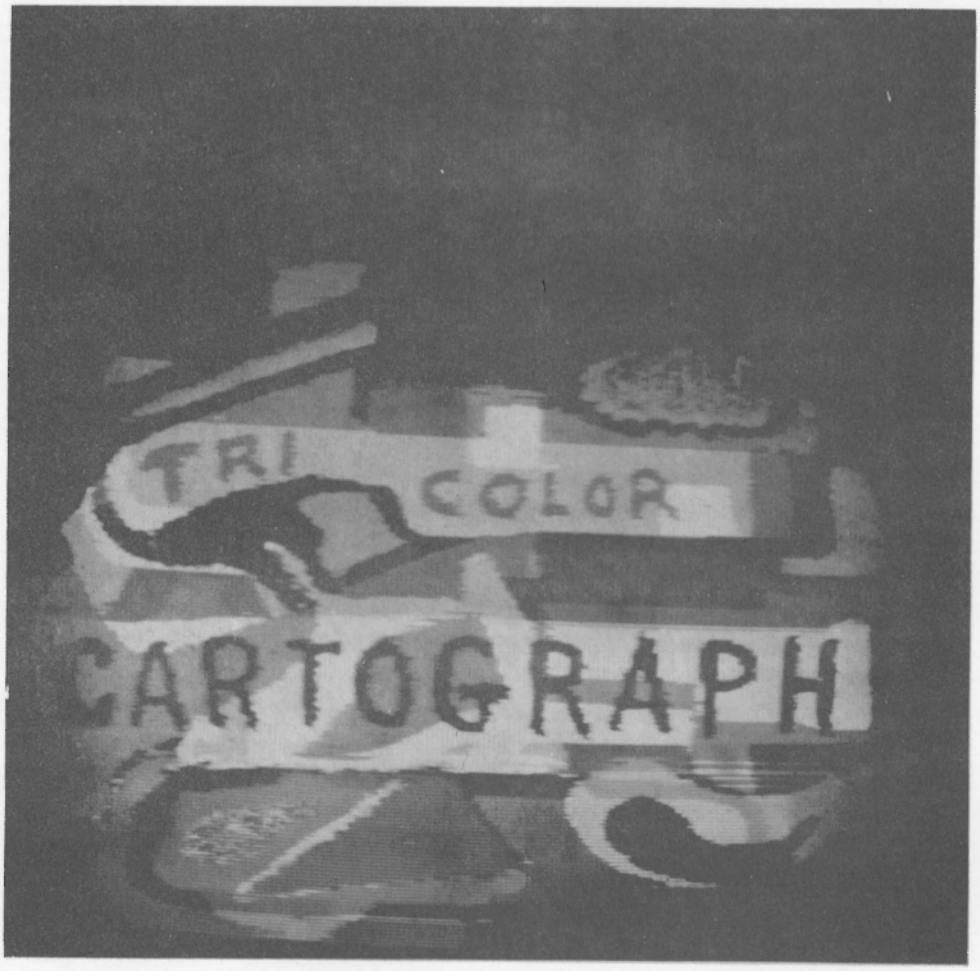


Figure 55. Photograph of Sample Artwork
(Original in Color)

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15. Supplementary Notes

16. Abstracts

This report describes improvements made on the Automatic Tricolor Cartograph - Mark I. The Cartograph is a self-contained system for performing the automatic coloring of operator-designated bounded areas on a color display. It has its own storage and refresh. In the original version, the storage of colored areas was such that striations were somewhat noticeable on the display. In addition, the only means of inputting outline information (to define the bounded regions) was by means of the light pen. Only saturated colors were possible.

The improvements described here were developed to eliminate the above 3 shortcomings of the original system. A demodulation scheme was developed to eliminate the striations. An input system using a television camera was developed so that line drawings can be input directly without using the pen. Finally, a scheme for linear writing was developed so that the 3 primaries can be varied in saturation.

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Television Graphics
Display Systems
Delay Line Differentiation

17b. Identifiers/Open-Ended Terms

17c. COSATI Field/Group

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